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Arnold A. Cohen

CHAIRMAN, 1960–1961

Arnold A. Cohen (A'42–M'47–SM'51) has been elected Chairman for the year 1960–1961 by the PGEC Administrative Committee.

Dr. Cohen was born in Duluth, Minn., in 1914. He received the B.E.E. degree in 1935, and the M.S. and Ph.D. degrees in physics in 1938 and 1947, from the University of Minnesota. His graduate research was in mass spectometry, ion optics, and related instrumentation techniques.

In 1942, he joined the Radio Corporation of America, where he engaged in electron tube development. He entered the digital computer field in 1946, when he joined the newly formed Engineering Research Associates, Inc., in St. Paul, Minn., which is now part of the Remington Rand Univac Division of Sperry Rand Corporation. In his present position as Engineering Director, System Planning, he directs advanced technical planning activities for the Military Engineering Division of Remington Rand Univac.

A number of developments in the computer field have been identified with Dr. Cohen, including development of basic magnetic drum storage techniques. He was responsible for the system design of the ERA 1101 and 1103 (Univac Scientific) computers. He is a co-author of the book "High Speed Computing Devices," and has been issued a number of patents in the data processing field.

Dr. Cohen was Chairman of the Twin Cities Section of IRE in 1951–1952, and spearheaded formation of the Twin Cities Chapter of PGEC in 1957. A member of the PGEC Administrative Committee since 1958, he was Vice-Chairman during the past year. In 1957 he served on the Technical Program Committee of the Eastern Joint Computer Conference, and in 1958 he was Publications Chairman. He was Vice-Chairman of the U. S. Technical Program Committee for the 1959 International Conference on Information Processing, and is currently serving on a Department of Defense scientific advisory panel.

Dr. Cohen is a member of Sigma Xi, Tau Beta Pi, Eta Kappa Nu, and the Association for Computing Machinery.

High Density Digital Magnetic Recording Techniques*

A. S. HOAGLAND† AND G. C. BACON†

Summary—The merit of any high density detection method is ultimately dependent on the "resolution" characteristic of the magnetic recording components. Justification of readback waveform synthesis through "single pulse" superposition is given. A comprehensive, yet general readback simulation program is described which will automatically, for any characteristic pulse, simulate all possible readback signal patterns and test them for specified reading logic as a function of bit density. Amplitude, phase, peak, etc., sensing are compared and the influence of parameter variation on performance indicated. Good correlation with experiment has been realized and has greatly reduced time at the bench. The significance of pulse waveform is clearly revealed and this study has provided a guide to head design (ring and probe), permitting the optimization of a total recording system for high-density storage.

Introduction

MAGNETIC recording of data involves the storage and processing of binary information, utilizing two states which are capable of being differentiated. For convenience, consider NRZ (non-return-to-zero) recording in which the storage surface is continuously saturated during writing, in one direction for a "1" and in the opposite sense for a "0." A particular input is then composed of a succession of alternating step changes in writing current. Reading involves a derivative-type action, as indicated schematically below, which illustrates the over-all transfer process from input to output. The surface co-ordinate is x, and $\bar{x}$ represents the variable indicating the position of the specified surface magnetization relative to the magnetic head.

$$\underbrace{i(t) \rightarrow M(x)}_{\text{writing}} \cdots \underbrace{\phi_h(\bar{x}) \rightarrow vNd\phi_h/d\bar{x}}_{\text{reading}} = e(\bar{x}) = e(vt) \quad (1)$$

where

$M(x)$ = distribution of magnetization recorded in the storage surface,
$\phi_h(x)$ = reading coil flux as a function of surface position,
e = open-circuit readback voltage,
N = number of turns on the reading coil,
v = surface velocity, and
t = time.

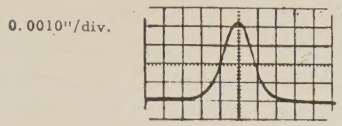
Hence, $e(vt)$ is a pulse-like signal for a step change in $i(t)$,[1] and the surface velocity appears as a scaling factor in both time and amplitude for the output signal. A output voltage signal is then associated with eac change in the direction of saturation or reversal in wri ing current.

Consider the output signals for arbitrary input pa terns consisting of sequences of alternating step-lik changes in writing current. On readback, the magnet field present, caused by the recorded magnetization the surface, is extremely weak and, hence, the magnet head will behave very nearly as a linear element. Wri ing definition, corresponding to the width of a saturatio transition region, is much less than the correspondin reading resolution because of the nonlinear surfa saturation characteristic.[1] Therefore adjacent chang in surface state will not modify one another even wit considerable pulse crowding. These considerations imp that the principle of superposition may be usefully a plied to the overall input-output transfer process in i vestigating high density recording with the use of th characteristic step function output response. The widt and waveform of this characteristic step function pul response, $e(x)$, are thus extremely important. Such r sponses will be shown as functions of x, or distance, as this manner they are most meaningful. Since the surfa magnetization will consist inherently of an alternati train of magnetization reversals, the readback wav form may be regarded as an alternating pulse sequenc As indicated in the foregoing, the velocity enters on as a scaling factor between distance and time. Accor ingly, bit density considerations may be derived direct from this type of analysis.

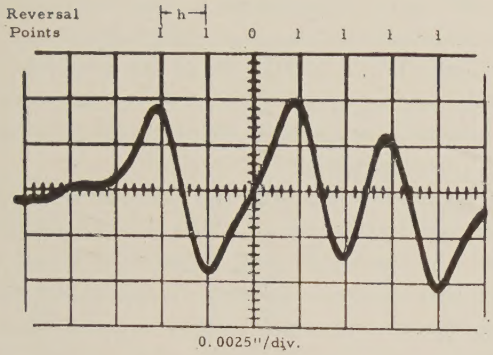
This superposition concept, as applied to digital ma netic recording, has been experimentally confirmed. an example, Fig. 1 shows a readback waveform resultin from a given sequence of magnetization reversals alon with the characteristic pulse of the system. This wav form is the signal waveform resulting from graphic superposition using $e(x)$. It is seen that the correspon ence is quite good. The minimum separation of ma netization reversals, $h_{\min}$, at which the use of superpo tion to predict output waveforms begins to break dow may be experimentally ascertained by noting the alte nation density at which a marked deviation between t actual readback waveform and that obtained fro graphical superposition commences. This point occu beyond the present operating limits for bit density (s by pulse crowding) with currently employed detecti techniques. Hence, the superposition concept is a pow ful tool for the exploration of high-density recordin

* Manuscript received by the PGEC, October 26, 1959; revised manuscript received, January 11, 1960.
† IBM Research Laboratory, San Jose, Calif.
[1] A. S. Hoagland, "Magnetic data recording theory: Head design," *Commun. and Electronics*, vol. 27, pp. 506–512; November, 1956.

tual factors causing perturbations of the recording stem may be included and the over-all detection aracteristics then examined.



(a)



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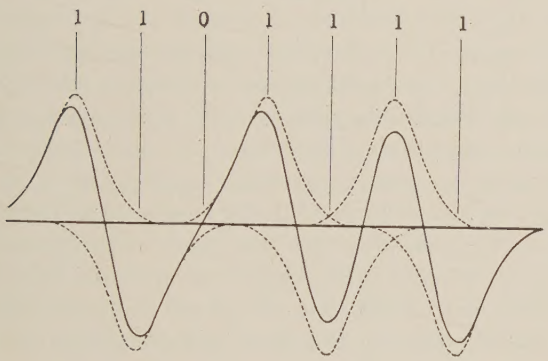

(c)

g. 1—Comparison of experimental and superimposed waveforms (1 = magnetization reversal). (a) Characteristic pulse $e(x)$. (b) Readback waveform. (c) Waveform resulting from sup erposition

The principle of superposition is employed, using $e(x)$, synthesize the readback waveform for arbitrary nary sequences. Then, to study the density potential various recording methods, each decoding procedure ust be tested against all possible waveforms that uld arise in a bit interval at each recording density; is examination must be continued as the density is creased until no error-free run is possible. The num- r of unique readback waveforms that may be en- untered in a bit cell is a function of the degree of inter- mbol interference, or pulse crowding, that may arise. or example, until h is chosen less than λ, the character- ic pulse basewidth, only one basic bit cell waveform ll arise. If the waveform synthesis procedure includes possible waveform patterns which result when up three adjacent bits on both sides of a given bit can produce pulse response interference with the signal of the given bit, *i.e.*, XXX-XXX, then this procedure insures that the "worst" case will be considered with this degree of potential intersymbol interference. This degree of bit interaction was used in the work reported here. The choice of three adjacent bits corresponds to a range for n (where n is the numbering of adjacent bit cells) of from -3 to $+3$ based on the expectation that the actual feasible density limits encountered for the detection techniques studies would not lie beyond the corresponding permissible range of "total" recording pattern simulation. Needless to say, this latter condition did exist. Note that if $e(x)$ has a basewidth of λ, then with $n=3$ the corresponding waveform synthesis is valid until a pulse in an $n=4$ cell would interfere with the test cell. Thus a maximum density of $7/\lambda$ alternations per inch can be simulated. This is three and one-half times the density at which recorded amplitude modulation, due to pulse crowding, commences to appear. If the density limit obtained with a given recording technique were to exceed $7/\lambda$ then the restriction on n_{max} would have to be modified to include provision for more extensive near-neighbor interaction.

The most common method of recording digital data is the NRZ method where either "1," "0," or a binary sequence change is represented by a step like reversal in current. Considered here is the version (NRZI) where the current is switched in direction each time a "1" is to be recorded. An output pulse is then associated with each recorded "1." We will first indicate the basic simulation method for two sensing schemes, amplitude sensing and peak sensing. These techniques enjoy considerable popularity as well as providing an illustration of the approach for two conceptually different methods to information detection, being predicted as they are on two entirely different signal waveform characteristics.

The simulation of waveform synthesis and the decoding process may be done on a digital computer. For the work here an IBM 650 computer program was developed wherein 40 points were used to represent a characteristic pulse signal. In addition, some very important operating considerations will be covered and the general utility of the program with respect to these practical aspects of recording will be demonstrated.

Amplitude Sensing

With NRZI recording the most common and direct method of detection is amplitude sensing where a "1" is indicated by the presence of a pulse and a "0" by the absence of a pulse. This detection method is inherently relatively insensitive to base-line "noise." Of particular interest then is: what is the maximum storage density to which such a detection means can correctly operate? An error will result when, at sample time, $|e(0)| > e_T$ or $|e(1)| < e_T$. Here e_T is a preset discrimination level, $e(0)$ is the output amplitude from a recorded "0" and $e(1)$ is the amplitude from a recorded "1." It should be appar-

ent that in providing an equal margin of protection against the two ways in which an error could arise, e_T may vary as a function of density.

An answer can be given fairly directly to the above question if the characteristic pulse is symmetrical and an impulse strobe is assumed. Let ρ represent the pulse width from the pulse peak to the point on either side at which the pulse amplitude is equal to $\frac{1}{3}$ the magnitude of the pulse peak.

Now first consider an isolated "1" in a binary sequence. Then at a density equal to $1/\rho$ the adjacent "0's" will provide a sample pulse signal equal to $\frac{1}{3}$ where the maximum signal amplitude of the waveform is considered normalized to "1." This situation represents the worst case (largest amplitude) that pertains to the detection of a "0" among all possible binary patterns. Then recalling that the pulse sequence must alternate, consider the central bit in an adjacent group of 3 "1"'s surrounded by zeros. The pulses corresponding to the outer "1"'s then subtract from the central pulse. Now at the density $1/\rho$ the signal level at sample time for the central bit is equal to $1-2(\frac{1}{3})=\frac{1}{3}$. This particular binary pattern again corresponds to the worst case for the detection of a "1."

Thus at a density equal to $1/\rho$ we are at the limit of amplitude discrimination detection and hence $1/\rho$ is the maximum possible density that could be expected with amplitude sensing. For example, for a triangular pulse of base width equal to λ,

$$\rho = \lambda/3 \tag{2}$$

or the maximum theoretical storage density is equal to

$$(bpi)_{\max} = 3/\lambda. \tag{3}$$

For this characteristic pulse model the limiting bit density with amplitude sensing is equal to the magnetization alternation density at which the roll-off curve (output amplitude vs magnetization alternation density) has dropped to $\frac{1}{3}$ of the maximum signal. The limitation here arises specifically from pulse crowding and sensing is predicated on the acceptance of considerable intersymbol interference.

Now in actual practice one must contend with considerable departures from this "first order" model. Then the computer program outlined below provides a flexible means to attack the general detection question with a high level of sophistication.

Upon readback, with amplitude detection, the signal waveform is strobed at the center of each bit cell (external clocking is assumed) and the sample value is compared with a preset discrimination level. For this work the strobe width is kept at $\frac{1}{5}$ of the *bit interval*. If the magnitude of the strobed signal sample is greater than this discrimination level, the sensing decision logic establishes the bit as a "1"; if the signal amplitude is less than this threshold level, a "0." The simulation program incorporates the requirement that the readback waveform sample exceed the "1" sense level for the full width of the strobe before the presence of a "1" is indicated. This serves as a criterion to provide for a reliability in actual circuit implementation.

There are limits at any given bit density between which this discrimination level must be set to allow the proper identification of each strobed sample. If this level is below an established lower limit, some "0"'s will be interpreted as "1"'s; if it is above an upper limit, some "1"'s will be detected as "0"'s. As the program considers "cell" signal waveforms arising from all possible patterns produced by varying the states of the 3 adjacent bit intervals on each side of the test bit, the determination of the upper and lower sensing level limits at any density involves the examination of all possible seven-bit code patterns.

With the center bit assumed written as a "1," the strobed signal amplitudes of this cell are used to determine the upper sensing level limit; if this test bit is a "0," the strobe samples are used to determine the lower amplitude threshold limit. Thus, for a given density, the upper limit would be the lowest-amplitude "1" signal obtained while the lower limit is equal to the maximum-amplitude strobed "0" signal. Fig. 2 shows the curves displaying these limits as a function of bit density with the characteristic pulse from which these curves were constructed. The crosshatched area shows the region in which the amplitude sensing level must be placed for error-free detection. Obviously this recording system would start to give errors with some patterns at 1075 bits per inch, at which point the sensing level limits intersect. A reduction in density below this figure (down to about 700 bpi) will permit an increasingly greater tolerance for variation in the sense level setting. One can note the effect of the overshoot and the asymmetry of this particular characteristic pulse on the sensing level limit curves (as well as on the patterns that caused the amplitude threshold limits at various densities). These limiting patterns are tabulated in Table I. In particular, note in Fig. 2 the rises in the lower sense limit at 600 and 1200 bpi due to the presence of pulses (which, again, possess overshoot) in the adjacent cells. The fall in the upper sensing level limit at low bit densities is due to the strobe intersecting the characteristic pulse away from its peak, since the strobe width is related to the bit interval rather than the pulse width.

This basic waveform synthesis and detection routine may now be extended by any further reading logic that one may wish to apply to the basic detection scheme, *i.e.*, logical correction,[2] self-clocking,[3] etc. In addition, the NRZI coding scheme may be modified to represent

[2] A. S. Hoagland, "A logical reading system for nonreturn-to-zero magnetic recording," IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-4, pp. 93–95; September, 1955.

[3] L. D. Seader, "A self-clocking system for information transfer," *IBM J. Res. Dev.*, vol. 1 pp. 181–184; April, 1957.

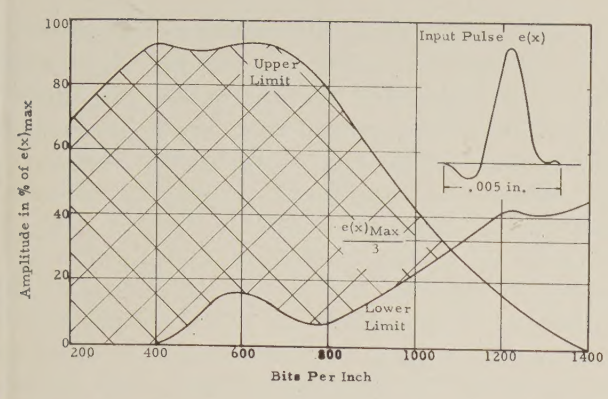

Fig. 2—Amplitude sensing level limit curves.

TABLE I

TEST PATTERNS THAT CAUSED THE SENSING LEVEL LIMITS OF FIG. 2

Bit Density (bpi)	Upper Pattern Test Position ↓	Lower Pattern Test Position ↓
300	0001000	1110111
450	0011000	0010100
600	0011000	0010100
750	0111110	0110010
900	0111110	1010010
1050	1011110	1000110

phase modulation scheme[4] as shown in Fig. 3. Here onreturn-to-zero recording is assumed with a positive ulse representing a "0" and a negative pulse represent-ig a "1." If two or more "1"'s are to be written con-ecutively the inherent alternating character of the mag-etization results in a signal output pulse of opposite olarity between the resulting "1" pulses. These "ex-raneous" pulses need not be sampled as they contain o new information, but nevertheless they will cause reater pulse crowding at any particular density and nus modify the strobed signal values. The same state-ients apply to a sequence of "0"'s.

The computer program allows a rapid comparison of ne relative advantages of the NRZ and phase modula-on schemes. Intuitively one sees that with phase mod-lation only the polarity of the sampled waveform need e considered; thus, the lower sense level limit is "0." sing the same characteristic pulse as in Fig. 2, the pper sense level limit as a function of bit (not pulse) ensity is shown in Fig. 4. The difference of the sense vel limits of the NRZ scheme of Fig. 3 is plotted along ith this, as this is an analogous measure of the signal mplitude tolerance of the sensing level setting. As ight be expected it is seen that the phase modulation urve falls off at just over half the density given by the RZ difference curve. In other words, the fact that the wer sense level can be near "0" does not compensate r the increased pulse crowding. This comparison does

[4] F. C. Williams, T. Kilburn, and G. B. Thomas, "Universal high-eed digital computers: a magnetic store," *Proc. IEE*, pt. II, vol. , pp. 94–106; April, 1952.

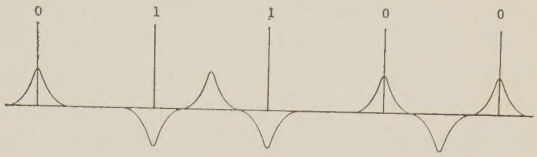

Fig. 3—Phase modulation readback signal (low density).

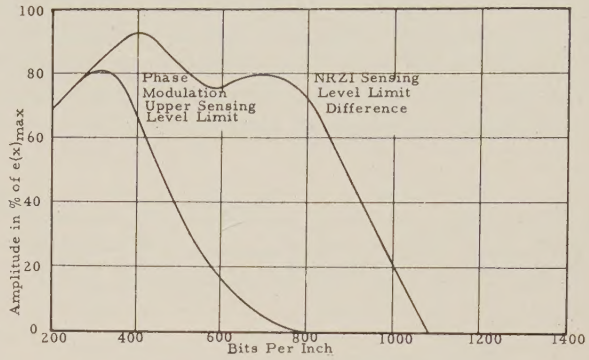

Fig. 4—NRZI Amplitude and phase modulation comparison.

not, of course, take account of possible advantages of the redundant pulses in error detection.

Further extensions of the basic amplitude sensing routine and uses of the sensing level limit curves will be shown later. In order to make subsequent relative comparisons of the influence of parameter variation on both amplitude and peak detection techniques, the peak sensing simulation program will first be described.

PEAK SENSING

The recorded step response typically results in an output pulse with a very high degree of symmetry about the peak. Then the peak, being centrally located, possesses the greatest degree of isolation (among all the sections comprising the waveform) with respect to intersymbol interference. Therefore the technique which intuitively seems obvious as a means to extend density in the face of pulse crowding is peak sensing. Inherently this method provides insensitivity to amplitude variation since it does not directly exploit this waveform feature.

In peak sensing, the detection problems are somewhat different as it is necessary to determine if a signal peak[5] of proper character occurred within a prescribed bit interval. Thus the readback waveform must be examined throughout the entire bit interval for the presence of such a signal peak.

Specific knowledge of the character of the actual intended peak detector is required to meaningfully simulate this detection method. In practice it would be undesirable to have a detector that would respond to every signal peak of the readback waveform as the system would then be susceptible to all noise peaks and base-

[5] More precisely, points where the derivative of the signal changes sign.

line ripple. In the work presented here, the detector represented in Fig. 5 was simulated. The low-pass filter network is merely for impulse-type noise elimination and does not cut off any significant part of the signal frequency spectrum. Hence, it is not involved in the detection simulation program since such noise is not generated and inserted in the computer signal waveform synthesis. The specific detector circuit treated requires that the computer program output representing the simulated differentiator *change polarity* and achieve a certain minimum magnitude before indicating the existence of a peak, as shown in Fig. 5.

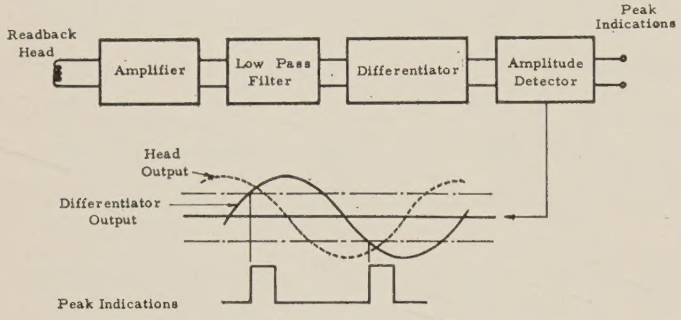

Fig. 5—Block diagram of peak detector.

From the discussion of the computer simulation of amplitude sensing it is easy to see how the same general procedure applies here. All possible seven bit patterns are again generated and the waveform in the center bit cell is examined for the above characteristics of detectability. As an "acceptable" peak is located, its spatial position within the bit cell is recorded as an output along with the associated bit pattern and bit density. If a signal peak should have been located in a bit cell but no peak is detected, or vice versa, a failure indication is noted.

If the system is externally clocked (*i.e.*, if the bounds of the bit interval are defined independently of the recorded information) the above type of failure completely determines the upper bit density limit. However, if due to timing variations self-clocking must be employed, a somewhat modified failure criterion must be used. Fig. 6 shows the type of self-clocking used in which the clock is rephased each time a peak is detected. If, as previously defined, the bit interval is h (*i.e.*, the maximum clock rate $= 1/h$) an error will occur for two successive "1"'s written mh apart (m is an integer) if the distance between the two resulting readback peaks, d_m, is not within the range

$$(m - \tfrac{1}{2})h < d_m < (m + \tfrac{1}{2})h. \qquad (4)$$

("0" peak shift is understood to imply $d_m = mh$.) If the lower limit is exceeded a "0" will be omitted in the readback binary pattern while a peak separation greater than the given upper limit will cause an extra "0" to be inserted in the decoded information.

It is now a relatively simple matter to scan the output list of peak locations within the test bit cell at a given density and determine the maximum magnitude of peak shift. Since the concern about peak shift with self-clocking relates to the relative separation between *successive pulses* it is necessary to determine the net shift by considering the effect on each pulse (treated as the test cell) within the context of the same code pattern. It became readily apparent that for a great variety of pulses with little or no overshoot[6] one particular pattern configuration always gave a failure as early, if not earlier, than any others. Fig. 7 shows this pattern and two ways that it may cause an error. In both cases the readback failure is caused by the shift of the readback peaks of two adjacent ones surrounded by "0"'s.

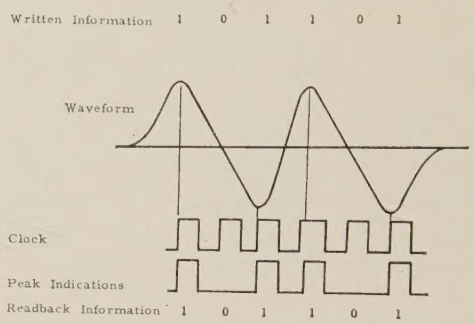

Fig. 6—Self-clocking logic.

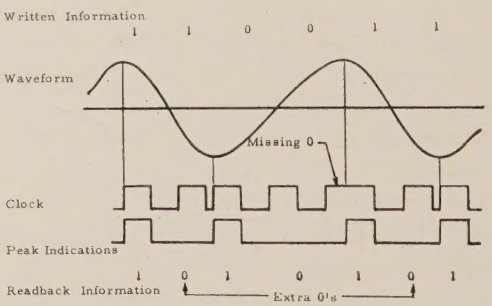

Fig. 7—Self-clocking failure situation.

One might initially suppose that a possible way to circumvent this problem and hence have a means to obtain a higher density would be to deliberately write the two "1"'s (*i.e.*, current reversals) closer together than the reference clock period, since this worst case can be recognized prior to recording. Experiment and graphical superposition show that this concept is not fruitful. Typically, a curve like that of Fig. 8 is obtained. For a bit interval greater than h_0 (see Fig. 8) there is negligible peak shift. However, as h is reduced (increasing the bit density) the peak separation rapidly approaches a fixed

[6] In general, characteristic pulses with significant overshoot cannot be used in a peak sensing system. If the detector indicates a peak when reading the overshoot, the system will automatically fail. For high-density recording the detector would need sufficient dynamic range to sense all but the smallest "unwanted peaks."

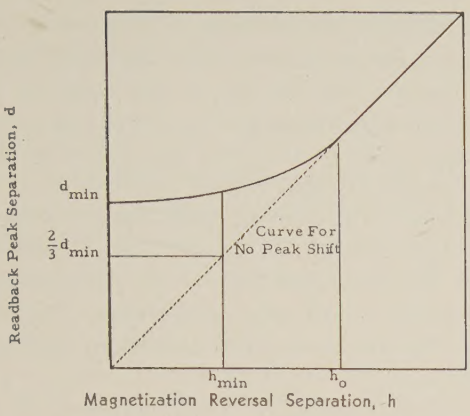

Fig. 8—Peak shift vs h for 00011000 pattern, where $bpi = 1/h$.

value d_{min}. In fact from (4)

$$h_{min} = \left(\frac{1}{1.5}\right) d_{min} = \left(\frac{2}{3}\right) d_{min}. \qquad (5)$$

Recall that $bpi_{max} = (h_{min})^{-1}$ so that $(bpi)_{max} = 1.5/d_{min}$. Predicated on the superposition concept, d_{min} can be readily interpreted as follows. Note that the readback waveform representing two successive "1"'s is obtained from the subtraction of the characteristic pulse, shifted by the distance h, from itself. In effect, one is approximating differentiation of the characteristic pulse through taking finite differences with interval h. In the limit as h goes to "0," then the peaks of the readback waveform approach a separation equal to the distance between the steepest slopes of the characteristic pulse, *i.e.*, the separation of the dipulse peaks of $\dot{e}(x)$, where $\dot{e}(x) = de(x)/dx$. To minimize peak shift these inflection points should be as near each other as possible; or in general one would like to have cusp-shaped characteristic pulses to most fully complement a peak sensing detection system.

A convenient way of representing the peak sensing density resolution allowed by a given characteristic pulse is to plot the percentage peak shift, 100 $(d_i - h)/h$ (where d_i is the peak separation arising from two adjacent ones), against bit density for the worst-case pattern group. This can be done quite rapidly by the computer. If the characteristics of the peak sensing circuit are reasonably simple, this is easily done graphically. Fig. 9 shows a characteristic pulse and the curve that results. On this same plot is shown a curve that was experimentally obtained from the recording unit that provided this characteristic pulse. The agreement between these two curves again confirms the engineering validity of the superposition approach to recording techniques analysis.

Consider the relative timing aspects of self- and externally-clocked systems that use peak sensing. With external clocking a peak may be anywhere within its appropriate bit interval. Thus for the worst case situation cited above, the peaks could be separated a maximum distance of 2 bit cells, while with self-clocking 1.5 bit intervals is the maximum separation that can be tolerated. Thus if the accuracy of the external clocking is perfect, self-clocking decreases the bit density potential by a factor of $\frac{3}{4}$. It is of interest to note that for an idealized triangular pulse it can be analytically shown (with self-clocking restrictions) that the limiting density due to peak shift is $3/\lambda$, or the same as obtained for this idealized pulse with externally clocked amplitude detection. This fact will point up the significance of considering operating factors (see below) in order to properly get an evaluation of detection methods.

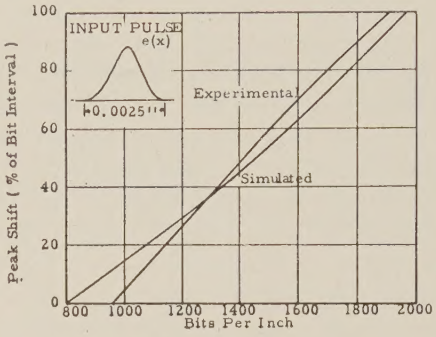

Fig. 9—Peak shift vs bit density.

Operational Considerations

The amplitude and peak sensing simulation procedures that have been described are basic tools whose extension to demonstrate the introduction of practical operating factors and parameter variations into a recording system analysis will now be described. As the over-all goal is the optimization of a recording system the limitations imposed by these factors must be understood.

Amplitude Perturbations

Most applications here of the computer programs exploit the linear characteristic of the readback model. For example, if the amplitude of the characteristic pulse is changed, the sensing level curves of Fig. 2 will be scaled by the same factor. This has direct application with amplitude sensing in the specification of manufacturing tolerances for the output of heads used in a memory where a group will feed the same detector, such as the heads of a drum that are individually selected and connected to a common read amplifier by some switching network. If the assumption is made that the characteristic pulse waveform of each head differs from any other only by a constant scaling factor, then each head will have sensing level limit curves that differ from those of the others by this scale factor. The object is now to determine the two composite sensing level limit curves as these alone are relevant to the single detector. The composite curves wanted are, of course, the highest lower limit curve and the lowest upper limit curve. As-

sume that the curves of Fig. 2 correspond to the head with the highest signal output. Then the lower limit curve here will be the lower limit curve of the composite set. The upper limit curve is that associated with the head of lowest output voltage. If, for a margin of reliability, we demand that the composite sensing level limit curves provide a threshold detection level range of at least 25 per cent of e_{max} at the operating density, the ratio of allowable head output variation may be obtained. That is, we can find the factor that must multiply the upper sensing level limit curve of Fig. 2 to cause the difference between the composite sensing level limits to be 25 per cent of e_{max} (at the selected operating density). If we record at a density of 800 bpi, using Fig. 2, this factor may be shown to be 0.41. Any lower ratio of lowest to highest head output would cause the sensing level limit difference to be less than 25 per cent of e_{max}. It should be noted that this same analysis can be used to determine the effects of small head-to-surface variations in which only the amplitude and not the general shape of the characteristic signal pulse is changed.

A problem very similar to the above arises when considering positioning tolerances for an access mechanism that moves a single magnetic head to cover a multiplicity of tracks (again assuming amplitude detection). As a head gives an output proportional to the width of the track that it is reading, any movement off-track gives a proportional decrease in the output from that track. Using this relation it is possible to show how the sensing level limit curves are modified as a function of the maximum access positioning error, $2P$. In Fig. 10 it may be

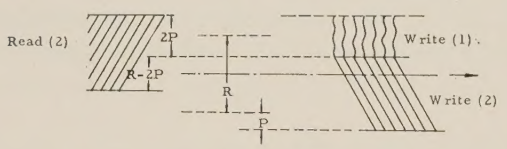

Fig. 10—Track misregistration problem.

seen how the "worst case" situation arises. The head, of track width R, first writes at a distance P to the right of a reference or true track centerline. The head is now considered on a later access motion to be located at a distance, P, to the left of this reference axis and new information recorded on the track. The worst case arises when the head is repositioned to read this track again but is assumed located off-track to the right again by the maximum distance, P, from the centerline. Here the smallest width of the desired (most recently written) information and the greatest width of the undesired or outdated information is read. The sensing level limit difference, Δ, will now be lowered by two factors. First Δ is reduced by the ratio of the last recorded path width (that is actually being covered by the head) to the head width. As is seen in Fig. 10, this fraction is $R-2P/R$. At the same time an uncrowded output pulse from the outdated recorded path provides the greatest potential additional decrease of Δ. The worst case corresponds to a pulse being previously recorded at the same track cell as the test bit but of the opposite polarity. Let the maximum upper sensing level limit of a single characteristic pulse be C (recall that the sense level limit is based on a finite width strobe). Then for the above worst case the upper sensing level limit will be reduced by a term equal to $(2P/R)C$ due to this factor. Likewise the lower sensing level limit can be increased by $(2P/R)C$ under worst case conditions. The following expression for the resultant minimum difference, Δ, may be written

$$\bar{\Delta} = \Delta \frac{(R - 2P)}{R} - \left|\frac{4P}{R}\right| C. \tag{6}$$

Or, if $\bar{\Delta}$ is specified, the maximum positioning error may be determined, *i.e.*,

$$P = \frac{R(\Delta - \bar{\Delta})}{2\Delta + 4C}. \tag{7}$$

Assume that we are using the recording system characterized by Fig. 2 and that a minimum $\bar{\Delta}$ of 25 per cent of e_{max} is required. If we are operating at 800 bpi it is seen that Δ is 70 per cent and C is 90 per cent of the characteristic pulse peak. Eq. (6) then gives a maximum tolerable positioning error of 0.09R.

As $C \geqq \Delta$, the maximum permissible value for P is obtained when $C=\Delta$ and $\bar{\Delta}=0$, *i.e.*,

$$P_{max} = \frac{R\Delta}{2\Delta + 4\Delta} = \frac{R}{6} = 0.167R. \tag{8}$$

Thus the allowable value of 0.09R, while small, is not too far from the maximum positioning tolerance value.

In general if there is an unwanted signal of a type that adds linearly to the readback waveform it may be dealt with in an analogous manner. Many times the worst case situations of the composite signal are obvious and through manipulations as simple as those above, direct evaluations may be made. If this is not the case it is still reasonably easy to have the computer automatically test all pertinent cases.

When peak sensing is to be employed, unwanted signals of the type described above pose a different problem. If the unwanted signal, by itself, will cause the detector to indicate a peak, then a detection failure will certainly result. The effects of any lesser disturbing noise signal must be superimposed on the signal waveform and the composite waveform examined. It is usually a computer problem to find worst cases as the resultant waveform must be examined in more detail than is the case with amplitude sensing. In a system in which the main perturbation is a variation in the readback waveform amplitude, peak sensing performance is only slightly affected, as the position of the signal peaks

is unchanged. In this respect it is considerably superior to amplitude sensing.

Clock Timing

Another operating condition quite readily handled by the programs is that of clock timing. All systems must tolerate a certain degree of clocking inaccuracy. When an external or fixed clock reference is used, some sacrifice in bit density must be accepted in order to tolerate timing variations; if the timing inaccuracy is potentially extreme, one is forced to employ self-clocking (with a likely restraint on code combinations to maintain proper circuit-surface synchronization).

The peak sensing computer routine is readily adaptable to this problem, since the indicated peak position within the bit interval is the program output. Thus it is simply necessary to determine the amount that the boundaries of the bit cell must be shifted to cause failure in the worst case. One half of this is the maximum allowable clock variation, as the total error has contributions from both reading and writing.

The externally-clocked amplitude sensing case is quite rapidly studied through a slight modification of the sensing level limit program. Again all seven-bit waveforms are constructed with the clock in the proper position. In the simulation of detection the strobe is moved both to the right and to the left in small increments. At each clock (*i.e.*, strobe) position, the upper and lower sensing level limits are noted, using all possible patterns. From these values composite sensing level limit curves as a function of clock shift are obtained for the density in question. If, for reliability, it is required that the sensing limits be separated by at least 25 per cent of e_{max} the above curve will establish the maximum allowable clock shift. Using the characteristic pulse of Fig. 2, plots of this maximum allowable shift are shown in Fig. 11 for both phase modulation and NRZ coding.

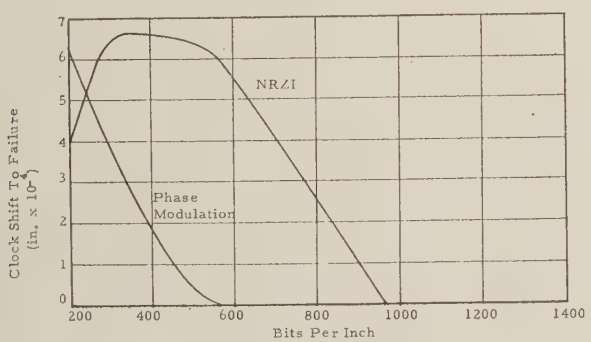

Fig. 11—Clock shift with amplitude detection.

The lower pulse crowding of the NRZ method is seen to be a favorable factor with respect to this problem.

The above applications have dealt with operational effects upon a system with a given characteristic pulse. Now we will look at the characteristic pulse itself to determine how it is related to the recording structure and hence the relation of head design to density.

Head Design

Through a reciprocity argument[1] a relation between $e(\bar{x})$ and $M(x)$ can be derived. In brief, if low-level excitation of the recording head produces a field distribution $H(x)$, then, based on the principle of reciprocity, the layer magnetization $M(x)$ at a depth y in the magnetic surface will produce a reading coil voltage $u(\bar{x})$ where

$$u(\bar{x}) = KvN \int_{-\infty}^{\infty} H(x) \frac{\partial M(x - \bar{x})dx}{\partial \bar{x}} . \qquad (9)$$

Here K is a constant and M and H are vectors combined by a scalar or dot product operation. If a ring-type head (or horizontal recording) is assumed, the significant component of the magnetization is in the x direction. Then, taking $M = M_x$ and for $M_x(x)$ a step function, the derivative of magnetization is an impulse and the above integral yields

$$u(\bar{x}) = u_x(\bar{x}) \propto H_x(\bar{x}); \qquad (10)$$

$u(\bar{x})$, the output signal waveform, is then proportional to $H_x(\bar{x})$.

Eq. (9) may be interpreted as analogous to a "scanning" process in which $H(x)$ is scanned by the distance derivative of the surface magnetization. When $M = M_x$ (and has a finite slope), $H_x(x)$ is scanned by a pulse-like magnetization function of finite width and the resultant $u(x)$ will have a broader and flatter waveform than $H_x(x)$.

For most practical cases $u(\bar{x})$ closely resembles $H_x(x)$ for a ring head and $u(\bar{x})$ resembles $H_y(x)$ for a vertical probe-type head.[7] Thus it is useful to have a method for determining $H_x(x)$ and $H_y(x)$ for a given recording environment. A rapid way to get estimates for these sensitivity or weighting functions, *i.e.*, H_x and H_y, is to use an electrolytic tank. Here an analogy is made between permeability and conductivity, and between H and E (electric field). For this purpose, the magnetic head is most easily regarded as possessing an infinite permeability. There is no concern about local saturation effects since this analog is to apply to readback analysis where very weak fields exist. The head is satisfactorily represented by a highly conducting boundary.

The saturated surface will not have a permeability significantly different from air and both can then be adequately represented by the electrolyte in the tank. Thus with the simulated head structure electrically excited, $H_x(x)$ and $H_y(x)$ can be found at any corresponding depth y in the "magnetic" surface. The total head "outsignal," $e(\bar{x})$, assuming a step change in M_x, is the con-

[7] W. Farrand, "An air-floating disk magnetic memory," 1957 WESCON Convention Record, pt. 4, pp. 227–230.

tribution from the entire surface, *i.e.*,

$$e(\bar{x}) = \int_{\text{over } d} H_x(x, y)dy. \qquad (11)$$

Here d is the surface thickness. This integral can be approximated by summing the contributions from several depths throughout the surface.

Then the characteristic pulse is determined by the head sensitivity function and the surface magnetization through the integral relation of (9). It is also evident that if the magnetization reversal is essentially step-like, the characteristic pulse very closely resembles the "mean" sensitivity function. This sensitivity function is easily obtained from an electrolytic tank or similar field analog, thus allowing a quick determination of the density limitation implications of a given head design. The above relationship allows one to predict the relative density performance of various head designs before construction is undertaken, thus being a considerable aid in guiding head design efforts.

Of particular interest, the above approach allows a quick relative differentiation between the properties of ring and vertical probe type structures. At the same head-to-surface spacing and with the same magnetic coating thickness, the dimensions of representative head types are chosen to each yield a sensitivity function of approximately basewidth, λ. Two such sensitivity functions for experimentally achievable designs are shown in Fig. 12 along with the corresponding recording geometry. Notice that the vertical probe head yields a sensitivity function with a flatter top and steeper sides than the ring head. This waveform dissimilarity between the ring and probe structures causes a pronounced difference in their sensing level limit and peak shift curves. The sensing level limit curves of Fig. 13 reflect the effects of the average slope of the sides of these readback pulses. When, for the probe head, the upper sensing level limit starts to fall at about 1000 bpi it falls very rapidly as the steep sides of the signal pulse would indicate (and similarly for the rise of the lower sensing level limit). The ring head, however, yields curves that fall off much more slowly and as a result would allow higher recording densities with amplitude detection than this probe head although their pulse widths are the same. The curves of peak shift shown in Fig. 14 demonstrate that peak sensing is even more critically dependent upon characteristic pulse shape. Intuitively this is substantiated by noting that the much sharper peak of the ring head sensitivity function will be distinguishable under greater pulse crowding than could be expected from the flatter top of the sensitivity function possessed by the probe head.

Surface Magnetization

The effects of a finite slope for the surface magnetization can now be estimated. The integral of (9) was

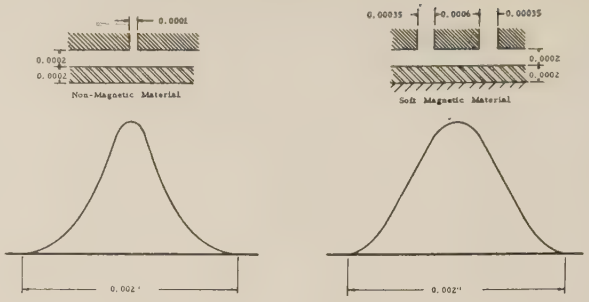

Fig. 12—Sensitivity functions.

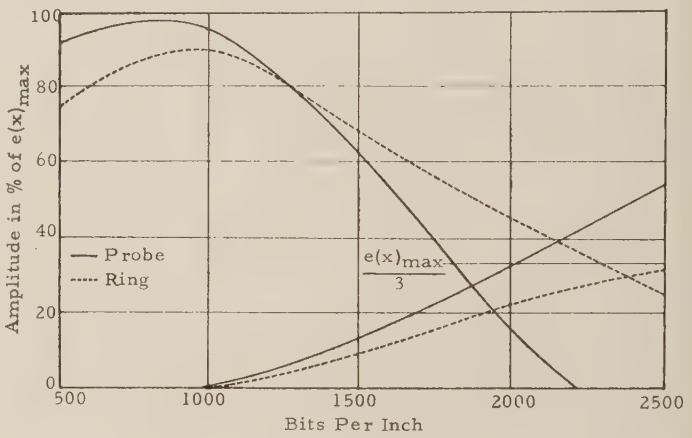

Fig. 13—Amplitude sensing level limit curves.

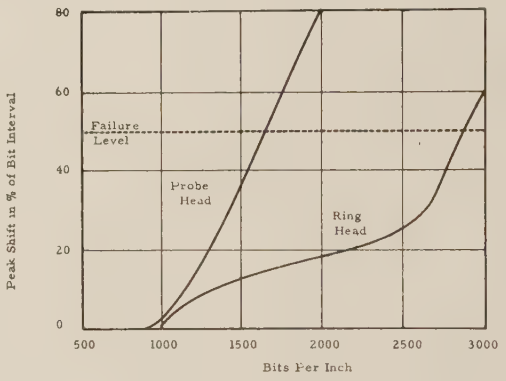

Fig. 14—Ring and probe peak shift characteristics.

solved graphically for a uniform magnetization reversal of $\lambda/5$ for both the ring and probe head discussed previously. This magnetization transition width places an expected upper bound on the applicability of superposition at $h_{\min}=\lambda/5$; for $\lambda=0.002''$, the maximum bit density that can be anticipated as susceptible to superposition simulation is 2500 bpi. The results of considering a finite magnetization change were characteristic pulse waveforms with broader bases and flatter peaks than those of the original sensitivity functions, as would be expected. In the comparisons of these results with the sensitivity functions, the probe sensitivity function is only very slightly modified while that of the ring is considerably changed. Neither the sensing level limit curves

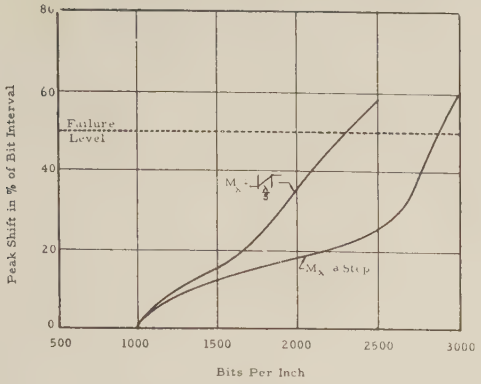

Fig. 15—Effect of M_x upon ring peak shift characteristics.

nor the peak shift curve were perceptably modified for the probe head. Likewise, the sensing level limit curves for the ring head were essentially the same. However, the peak shift of the ring head was considerably increased due mainly to the difference in the shape of the peak of the pulse. This increase in peak shift may be seen in Fig. 15.

Thus when peak sensing is to be used in conjunction with a ring-type head, efforts to obtain a magnetic surface that will sustain a narrower magnetization reversal may be worthwhile, this being indicated by the waveform difference between the characteristic pulse and the sensivitity function. Use of the sensitivity function itself in examining bit density limits corresponds to assuming an ideal surface, since true step changes in magnetization are assumed. Hence curves obtained in this manner indicate the range of potential gain that may result from improvements in the magnetic surface or in writing for a given detection technique. The data here are for a 200 microinch head-to-surface spacing. Closer spacing would tend to increase the significance of the surface in the over-all recording process.

Conclusions

The purpose of this paper has been to demonstrate the considerable amount of information relative to magnetic recording system performance that can be derived from the utilization of the characteristic pulse waveform. Both theory and experiment have demonstrated that the utilization of the superposition concept is valid beyond the range of recording bit density that is achievable for the detection techniques and head designs here. The waveform superposition synthesis has been advantageously simulated on a digital computer along with detection techniques and operational effects.

It is significant to note that the detection methods studied are very sensitive to the exact shape of the characteristic pulse. The pulse base-width, λ, is only one parameter characterizing this waveform and, as was shown in the comparison of ring and probe heads, it is not necessarily the most important. It was further shown that these pulse shape factors are more critical in peak sensing than in amplitude sensing. Hence this work has provided a means to interrelate head design and recording techniques to achieve over-all recording system optimization. Further, such analyses have given insight into the role of the magnetic surface in setting performance.

The computer programs will very suitably predict recording system performance and have greatly reduced exploratory bench work. The study here, while highlighting the nature and features of digital recording is primarily a valuable "tool" since, in itself, the simulation analysis does not directly produce new detection principles.

The Optimal Organization of Serial Memory Transfers*

ARTHUR GILL†

Summary—**This paper is concerned with the optimal compilation of programs whose function is to transfer words of information from one location in a serial memory to another. The most important optimization tool is the "timing schedule," which facilitates the analysis of various transfer schemes and the determination of the fastest one. The procedure described for optimizing serial transfers is readily programmable for computer execution, and is directly applicable to a general class of transportation problems.**

Introduction

A LARGE number of small-scale general-purpose digital computers currently in use are equipped with a high-speed memory of the so-called "serial" type. Examples are the IBM 650, Bendix G-15, Royal McBee LGP-30, and Datatron 205. The serial memory, in general, consists of a rotating magnetic drum, divided into a fixed number of peripheral channels, or "lines;" each line is able to hold a fixed number, say n, of serially recorded "words" of information. The information can be read from the drum, or recorded on it, by physically-stationary ferromagnetic heads; consequently, a specific word is accessible only once per drum revolution, or once every n "word-times."

The problem under discussion is that involving successive transfers from one memory location to another. To transfer a word from a location corresponding to word-time t to a location corresponding to word-time t', the following commands have to be issued: 1) read the "source line" into the accumulating register at word-time t; 2) record the accumulating register on the "destination line" at word-time t'. In the usual case, which will be assumed here, the capacity of the accumulating register is a single word, so that only one word can be transferred at a time.

In programs involving a large number of successive transfers, and where the over-all speed of operation is at a premium, it is imperative to select judiciously the sequence of transfers so as to minimize the wasted motion. In the following sections a systematic method will be described which facilitates the evaluation of various transfer sequences and the determination of the optimal one.

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The Timing Schedule

Prior to program compilation it is advantageous to display schematically the relative locations of the "source words" and the "destination words" as they appear in the memory. This is done in Fig. 1 for a program involving the successive transfers of 7 words in a memory where $n=20$. The source words and destination words are shown in two separate lines although, physically, they may be arbitrarily distributed among all the memory lines. The arrows point from the source words i ($i=2, 3, 8, 9, 12, 14, 18$) to the corresponding destination words, labeled i'. Also indicated are the entry word (denoted N), where the transfer program starts, and the exit word (denoted X), where the program terminates. To count the number of word-times between any two words, say i_1 and i_2, it is necessary to proceed from i_1 to i_2 in the shown "direction of travel;" if i_2 is numerically smaller than i_1, it is necessary to go through word 20 and then back to 1.

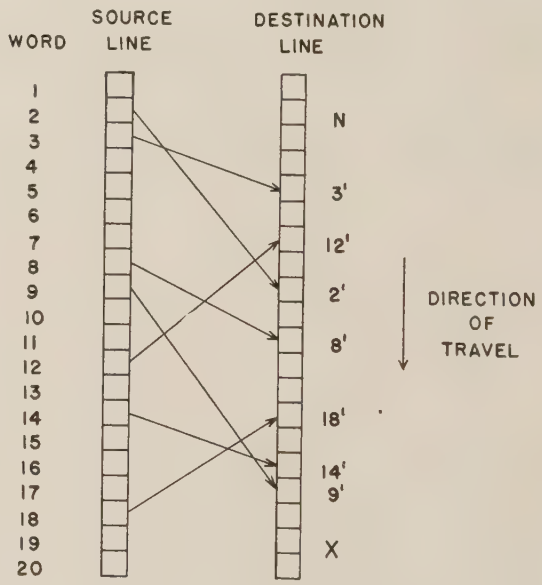

Fig. 1—A serial transfer problem.

It is convenient to visualize the accumulating register as a vehicle traveling parallel to the memory lines, alternately "loading" and "unloading" information words at preassigned locations. In these terms, the problem at hand can be formulated as follows: given the starting point N and the end point X, in what order should the

vehicle transfer the given words so as to minimize the total length of the route?

It should be pointed out that, in general, there is a fixed minimum number of word-times which have to be allowed before any reading and recording (or loading and unloading) operations can be performed. This number, denoted by r, equals the number of word-times required to execute a command in the given computer.

The timing information displayed schematically as in Fig. 1 can be concisely and effectively presented in a table which will be called the "timing schedule." In this $m+1$ by $m+1$ schedule, m being the number of source words, the first row and column correspond to word N and word X, respectively; the remaining rows and columns correspond to the m source words, arranged in their serial order. The elements t_{ij}, common to row i and column j in the schedule, are determined according to the rules listed in Table I (every rule in the table takes precedence over all following rules).

TABLE I

Element	Element Equals Number of Word-Times		
	Starting at Word	Ending at Word	Via Word
t_{NX}	—	—	—
t_{Nj}	N	$j-r-1$	—
t_{iX}	$i'-r$	X	i'
t_{ii}	$i-r$	$i'-r-1$	i
t_{ij}	$i'-r$	$j-r-1$	i'

Fig. 2 is the timing schedule for the problem depicted by Fig. 1, with $r=1$.

	X	2	3	8	9	12	14	18
N	—	19	0	5	6	9	11	15
2	12	7	14	19	20	3	5	9
3	16	17	2	3	4	7	9	13
8	10	11	12	3	18	21	3	7
9	4	5	6	11	8	15	17	21
12	14	15	16	21	2	15	7	11
14	5	6	7	12	13	16	2	2
18	8	9	10	15	16	19	21	15

Fig. 2 —The timing schedule for problem of Fig. 1.

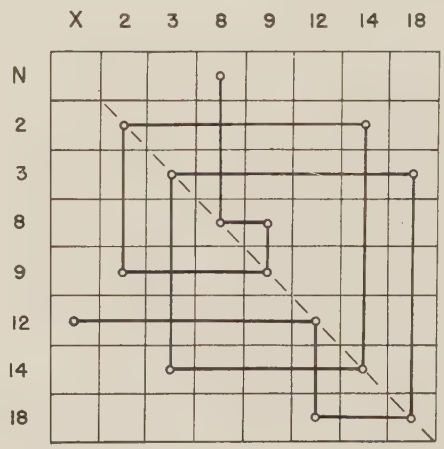

Fig. 3—A representation of the route N-8-9-2-14-3-18-12-X.

Applications of the Timing Schedule

The calculation of "route lengths" corresponding to various transfer sequences is greatly facilitated by the timing schedule. In general, to calculate the time required to transfer words $a, b, c, \cdots, m-1, m$ to $a', b', c', \cdots, (m-1)', m'$, in that order, one should mark the following schedule elements:

$$Na, \quad aa,$$
$$ab, \quad bb,$$
$$bc, \quad cc,$$
$$\cdots\cdots$$
$$(m-1)m, \quad mm,$$
$$mX.$$

The sum of the marked entries equals the route length in word-times.

As an example, Fig. 3 shows the representation of the sequence N-8-9-2-14-3-18-12-X on the schedule of Fig. 2. The marks, or "vertices," are shown with a set of straight line segments connecting each diagonal vertex with two off-diagonal vertices, and forming a continuous path between the vertex in row N and the vertex in column X. Summation of the marked entries, or the "weights" associated with the vertices, yields the total route length of 138 word-times. Generalizing, any specified sequence can be uniquely represented by $m+1$ off-diagonal vertices having the following geometrical properties: 1) every row and every column contains exactly one off-diagonal vertex, 2) when every off-diagonal vertex is connected by straight lines to the diagonal vertices on its row and column, a single continuous path is obtained which connects all the $2m+1$ vertices. The set of $m+1$ off-diagonal vertices featuring these properties will be called a "proper set." Thus, every proper set corresponds to a realizable route, and vice versa.

In terms of the timing schedule, the optimization problem can be formulated as follows: it is desired to find a set of m diagonal vertices and a proper set of $m+1$ vertices, such that the sum of the associated weights will be minimal. However, since the weights associated with the diagonal vertices are common to all possible routes, the problem simplifies to the following: of all proper sets of vertices, find the one whose total weight is the minimum.

A Minimization Procedure

Consider a timing schedule where, in each row, an off-diagonal element is circled, and call the circled element in row i the "weight of row i." A configuration of $m+1$ circles produced in this manner, with the total weight W, will be called a "W configuration." Circling the minimal off-diagonal element in each row results in a configuration whose weight is minimal. This weight will be denoted by W_0; larger weights will be denoted by W_1, W_2, $\cdots$ where $W_{k+1} = W_k + 1$.

The proposed minimization procedure is based on the fact that if all the W_0, W_1, W_2, $\cdots$ configurations are successively produced, then the first configuration encountered which constitutes a proper set of vertices is also the proper set whose total weight is the minimum. The formation of all the W_k configurations can be carried out by the following recursive procedure (initially $k=1$):

1) Test if the weight of any row in any of the W_j configurations previously formed ($j=0, 1, \cdots, k-1$) can be increased by $W_k - W_j$ by shifting the circle to another column. If so, perform the shifting and call the new configuration a W_k configuration. If not, proceed to step 3).

2) Test if any of the W_k configurations constitutes a proper set of vertices. If so, this set, augmented with m diagonal vertices, corresponds to the desired minimal route. If not, proceed to step 3).

3) Add 1 to k and return to step 1).

The described procedure is certainly preferable to exhaustive enumeration and examination of all possible routes, since the first proper set discovered by the procedure is guaranteed to yield the minimal route. With straightforward enumeration, on the other hand, no route is guaranteed to be minimal until the enumeration is completed.

As an example, Fig. 4 shows the W_0 configuration ($W_0 = 25$) for the schedule of Fig. 2. W_1 configurations can be produced by increasing the weight of row 3, or 9, or 18 by 1. The last alternative results in a configuration which constitutes a proper set of vertices, as shown in Fig. 5. Fig. 6 presents the corresponding minimal route, from which the optimal sequence N-3-8-14-18-2-12-9-X can be deduced. From the timing schedule the length of the minimal route can be calculated to be 78 word-times. This route is seen to be a considerable improvement over a route such as N-2-8-9-18-14-12-3-X, whose length is 198 word-times.

The following bounds are useful for estimating the amount of improvement which is possible by the above minimization process. $L_{\min}$ is the length of the minimal route; t_i is the minimal off-diagonal element in the ith schedule row:

$$\sum_i (t_{ii} + t_i) \leqq L_{\min} \leqq 2n(m+1).$$

These bounds can be strengthened by adding the requirement that $L_{\min}$ modulo n has to be equal to the number of word-times between N and X (inclusively). For the example of Fig. 2 we have:

$$78 \leqq L_{\min} \leqq 318.$$

The route of Fig. 6, then, is the minimal realizable for the specified set of t_{ii} and t_i.

	X	2	3	8	9	12	14	18
N	–	19	(0)	5	6	9	11	15
2	12	7	14	19	20	(3)	5	9
3	16	17	2	(3)	4	7	9	13
8	10	11	12	3	18	21	(3)	7
9	(4)	5	6	11	8	15	17	21
12	14	15	16	21	(2)	15	7	11
14	5	6	7	12	13	16	2	(2)
18	(8)	9	10	15	16	19	21	15

Fig. 4—The W_0 configuration for schedule of Fig. 2.

	X	2	3	8	9	12	14	18
N	–	19	(0)	5	6	9	11	15
2	12	7	14	19	20	(3)	5	9
3	16	17	2	(3)	4	7	9	13
8	10	11	12	3	18	21	(3)	7
9	(4)	5	6	11	8	15	17	21
12	14	15	16	21	(2)	15	7	11
14	5	6	7	12	13	16	2	(2)
18	8	(9)	10	15	16	19	21	15

Fig. 5—A W_1 configuration for schedule of Fig. 2.

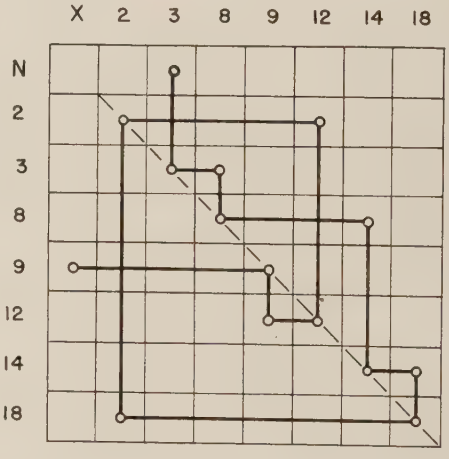

Fig. 6—The minimal route for problem of Fig. 1.

Conclusions

The ideas and techniques presented in the preceding sections are useful in improving the performance of automatic program compilers. The proposed minimization procedure can be easily programmed for computer execution and serve as an accelerating routine in such compilers. It should be pointed out that some past or future serial machines may have a different set of constraints from the one assumed here; however, these variations may only affect the rules governing the construction of the timing schedule (such as listed in Table I), but not the application of this schedule for analyzing transfer schemes and minimizing them.

The particular programming problem discussed in this paper is representative of a more general problem of optimizing the transportation of passengers or merchandise along a weighted route. This problem, known in the operations research literature as "the traveling salesman problem," has not yet been completely solved, although solutions are available for the special case (not applicable to our problem) of symmetric timing schedules.[1,2] The algorithm described above is partly based on the semisystematic scheme described in Sasieni, Yaspan, and Friedman.[2] Complete systematization is clearly essential if the scheme is to be useful for large timing schedules or if the scheme is to be incorporated in automatic program compilers, as proposed.

[1] C. W. Churchman, R. L. Ackoff, and E. L. Arnoff, "Introduction to Operations Research," John Wiley and Sons, Inc., New York, N. Y., pp. 470–472; 1957.
[2] M. Sasieni, A. Yaspan, and L. Friedman, "Operations Research-Methods and Problems," John Wiley and Sons, Inc., New York, N. Y., pp. 264–267; 1959.

The Design of Diode-Transistor NOR Circuits*

DALE P. MASHER†

Summary—**Considerations leading to the adoption of diode-transistor NOR circuitry for a moderately fast data-processing system are outlined. The design of the basic circuit is treated in detail. Development of a unique set of compatible logic packages from the basic circuit is described. This set is unique in the sense that a single type of diode-transistor circuit is used to provide the great majority of logic and storage functions required in the system. This single circuit type, which functions as a NOR circuit, is embodied in two package types. One package provides a single gate with a fan-in of five. The other package provides two gates, each with a fan-in of two. The latter type may be externally connected to provide a set-reset flip-flop. Only two other package types are used. The first is a passive transfer circuit which greatly simplifies shift register logic, and the second is a delay package which is closely related to the basic NOR circuit.**

Introduction

IMPLEMENTATION of a special purpose data-processing system for the Air Force required the design of a compatible set of solid-state logic circuits. During the study phase of the project, a number of feasible logic structures were considered for possible use in the equipment. The structures considered included the following:

1) Resistor transistor logic[1] (RTL)
2) Direct-coupled transistor logic[2] (DCTL) and several modifications thereof
3) Complementary transistor logic[3]
4) Current-steered logic[4]
5) Diode-transistor logic[5]

In addition to the logic structure, it was necessary to decide whether dynamic or static logic was to be used, and whether the circuitry would be synchronous or asynchronous. A decision was also required on a package design which would permit economical assembly and construction.

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[1] W. D. Rowe, "The transistor NOR circuit," 1957 WESCON Convention Record, pt. 4, pp. 231–245.
[2] R. H. Beter, W. E. Bradley, and R. B. Brown, "Surface barrier transistor switching circuits," 1955 IRE Convention Record, pt. 4, pp. 139–145.
[3] R. H. Baker, "Boosting transistor switching speed," *Electronics*, pp. 190–193; March 1, 1957.
[4] H. S. Yourke, "Millimicrosecond transistor current switching circuits," IRE Trans. on Circuit Theory, vol. CT-4, pp. 236–240; September, 1957.
[5] For a comparison of two types of DTL circuit see W. B. Cagle and W. H. Chen, "A new method of designing low level, high speed semiconductor logic circuits," 1957 WESCON Convention Record, pt. 2, pp. 3–9.

As a starting point, quasi-synchronous,[6] static logic was selected for the system. Two facts bear out this decision:

1) The static system lends itself to step-by-step checkout of dc levels not possible in the dynamic system, and
2) Synchronous circuits are simpler than asynchronous in the sense that they do not require the generation of special end-of-operation signals to initiate a succeeding operation.

Selection of a Logic Structure

The speed at which the logic circuits were required to operate was relatively low (*i.e.*, a 200-kc pulse rate was considered adequate). Therefore, logic schemes which use large numbers of transistors to achieve high speed of operation were rejected in order to minimize the total component count. Complementary transistor logic and current-steered logic fall in this class. Although DCTL systems are not noted for high speed, they require a single transistor for every logic input. In order to reduce the total transistor count, direct-coupled transistor logic was also rejected. For maximum circuit economy at the moderate speeds contemplated in these equipments, two types of logic structure proved outstanding. These structures were the RTL and DTL types.

Diode-Transistor Logic

Diode-transistor structures received considerable attention, both in paper studies and breadboard tests. In those circuits where a diode gate precedes a common collector stage, the transistor never enters its saturated region. Therefore, operating speed is not limited by transistor saturation effects. However, a common collector circuit provides neither logical inversion nor voltage gain. Hence, additional circuits, such as squaring amplifiers, inverters, and flip-flops, are required in addition to the basic gate. These additional circuits complicate the reliability and replacement problem. Because the transistor does not saturate, noise margins are lowered, and collector dissipation is seriously limited at high ambient temperatures.

A logic structure wherein the diode gate precedes an inverter, or common emitter transistor, has much to recommend it. With this type of structure, one standard configuration can satisfy all the logic and storage requirements of the entire system. Because the transistor is either saturated or cut off, noise sensitivity and power dissipation are minimized. Although the transistor saturates, the speed degradation occasioned by transistor storage time is not significant at the modest speeds contemplated here.

[6] The term quasi-synchronous implies that a clock is present and used to synchronize the logic. Not every logic package is clocked. Rather, the clock is used to synchronize a group or block of packages.

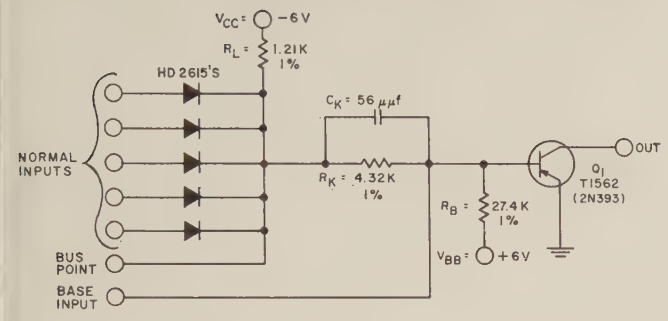
Resistor-Transistor Logic

Resistor-transistor logic, though simple and reliable in a component sense, is slower than diode-transistor logic. In common with the inverting type of DTL, one standard RTL configuration is sufficient for the synthesis of any conceivable logic or storage requirement. In fact, the problems attendant to diode gates preceding an inverter apply equally well to the RTL configuration. By substituting resistors for diodes, some measure of component reliability is achieved at the expense of storage time delay. This delay, in fact, is so large with commercially available alloy type transistors that 200-kc operation is doubtful. Some diffused base transistors are available with storage time delays compatible with 200-kc or higher operation. Those which show satisfactory saturation resistance and current gain, however, are not yet competitive in price and availability with the diode, alloy transistor combination. Furthermore, the RTL structure does not really utilize the maximum frequency capabilities of the transistor employed. A transistor capable of one speed in the RTL configuration may be capable of speeds up to ten times as fast in optimized diode-transistor configurations. Finally, the comparative inferiority of the RTL structure at high temperatures (because of the temperature induced increase in stored base charge) further militates against its use in this specific application. On the basis of all these considerations, the diode-transistor structure which incorporates the transistor as an inverter was selected as the most suitable type for use in the final equipments.

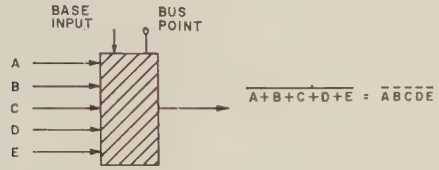
Design of the Basic NOR Circuit

Having indicated the reasoning involved in the selection of the logic structure, it is appropriate to consider the factors bearing upon the design of the basic circuit and the selection of its individual components. The diode gate preceding the transistor inverter receives first attention. This gate may be either of two types—a positive AND gate or a positive OR gate. Use of the latter type, as shown in Fig. 1(a), offers some advantage.

In order to demonstrate the advantage of the OR gate, it is necessary to consider the action of the RC coupling network which appears in the base circuit of Q_1. The resistor R_k is employed to limit base current and hence limit the depth of transistor saturation. The capacitor C_k across R_k improves the transient performance at the output. This capacitor supplies transient overdrive when the transistor is turning ON, and stores sufficient charge during the ON period to cancel the charge stored within the saturated transistor. This charge cancellation is possible because any input at ground potential allows the capacitor to discharge through a forward biased diode, the grounded input, and the base emitter circuit of Q_1. Had a positive AND gate



(a)



(b)

Fig. 1—(a) The basic NOR circuit and (b) its logic symbol.

been used, charge cancellation by means of a speed-up capacitor would be ineffective, since a capacitor in the position shown in Fig. 1(a) would be unable to discharge through diodes connected in the reverse of those shown. The positive AND structure would also permit an undesirable variation in the degree of transistor saturation, the depth of saturation depending directly upon the number of inputs which are negative and supplying base current. Correspondingly larger hole storage effects would be observed under these conditions. For these reasons, the positive OR gate was selected to precede the inverter. With this type of input, the basic circuit is conveniently described as a NOR circuit. That is, the output is the negated OR function of the inputs. The circuit, or gate, should not be viewed as a pulse source, but as a current sink. The output is either a high impedance to ground, or a low impedance to ground. The low-impedance state is defined as the ONE state. Thus a ONE on any or all inputs results in a ZERO or high-impedance output.

Supply voltages were selected rather arbitrarily, the choice being restricted by the permissible voltage range of the transistor used. Voltage levels of +6 and −6 were chosen because they are convenient values which permit low power dissipation within the transistor and provide adequate signal levels. The positive supply is used principally to supply reverse bias to the transistor through the resistor R_B. This reverse bias reduces the leakage current in an OFF transistor to an absolute minimum, and thereby reduces the OFF state power dissipation to a corresponding minimum.

The remainder of the design procedure consists of determining values and tolerances for the components R_L, R_K, C_K, and R_B, and of establishing a separate specification for the diode and transistor. The problem is considerably simplified by setting some boundaries within which to work. Experience has shown that a fan-in and fan-out ratio of five will usually provide directly for more than 80 per cent of a given system's requisite logic functions. Accordingly, we will attempt to choose the remaining parameters such that a fan-in and fan-out of five are achieved. With this fan-out, the maximum current carried by any one transistor will be

$$I_{\max} = \frac{5V_{CC}}{R_L}. \tag{1}$$

One of the limiting factors on the operating speed of the final circuit will be the rate at which system and stray capacitances can be charged and discharged. On this basis, it is desirable to make R_L as small as possible. In order to stay well within the current limitations of the transistor, however, R_L must be maintained at a reasonable value. In this case, a value of $1.21K$ was selected, permitting the maximum collector current for 5 loads to be 25 ma, a value equal to half the manufacturer's maximum rating for the selected transistor.

The values selected for R_K and R_B determine the driving capabilities of the circuit. Two stable states must be considered—the OFF state and the ON state. The OFF state equivalent circuit is shown in Fig. 2. In this state the transistor is being held OFF by an input nominally at ground potential. The actual potential at the diode bus point is the sum of a diode forward voltage and the driving transistor's saturation voltage.

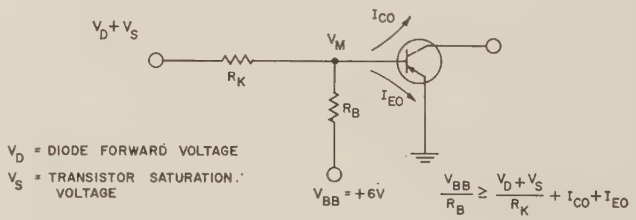


Fig. 2—OFF-state equivalent circuit.

This negative voltage must be counteracted by the positive voltage supplied from V_{BB} through R_B. For the transistor to be OFF, the base voltage V_M must be greater than or equal to zero. When this requirement is expressed in terms of the parameters shown in Fig. 2, we obtain the following inequality:

$$\frac{\overline{V}_{BB}}{\underline{R}_B} \geq \frac{\overline{V}_D + \overline{V}_S}{\underline{R}_K} + \overline{I}_{CO} + \overline{I}_{EO}. \tag{2}$$

The underlines and overlines are discussed below.

Fortunately, the right-hand side of the inequality contains factors which partially compensate for one another under changes of ambient temperature. The diode forward voltage decreases roughly at the rate of 2 mv per degree C, whereas the collector and emitter leakage

currents will roughly double every 8°C. Thus one term decreases while the other term increases. Eq. 2, therefore, in conjunction with the temperature behavior just noted, represents one constraint upon the selection of R_B and R_K.

A second constraint is imposed by requirements of the ON state. The ON state equivalent circuit is shown in Fig. 3. In this state, the transistor is held ON by one or more inputs which are nominally open circuits. In actual fact, the leakage to each collector which connects to an input drains off some of the current which could be used for holding the transistor ON. In each case, these collectors could be driving other gate inputs as well. Where these other gates are diode-coupled, additional current may be drawn away from the ON transistor to supply the leakage current of the diodes.

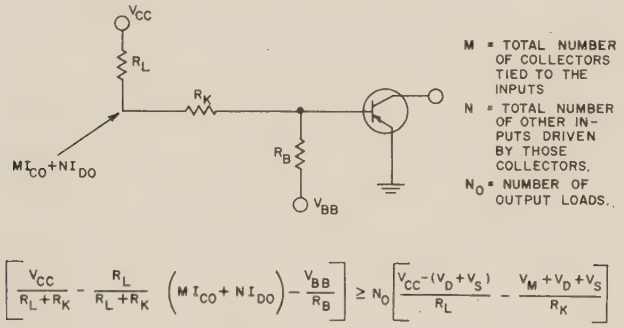


Fig. 3—ON-state equivalent circuit.

If M is the total number of collectors tied to the inputs, and N is the total number of diode inputs driven by those collectors, then $MI_{CO}+NI_{DO}$ represents the total negative leakage current at the diode bus point. In Fig. 3 this current is represented as a current source feeding the diode bus. This representation is valid since the individual leakage currents are relatively independent of the bus point voltage. Expressing the condition that the available base current times the minimum current gain of the transistor be greater than the load current, we arrive at the inequality

$$\underline{\beta}\,\frac{\underline{V_{CC}}}{\overline{R}_L+\overline{R}_K}-\frac{\overline{R}_L}{\overline{R}_L+\overline{R}_K}\left(M\overline{I}_{CO}+N\overline{I}_{DO}\right)-\frac{\underline{V_{BB}}}{\overline{R}_B}$$
$$\geq N_O\left[\frac{\underline{V_{CC}}-(\underline{V_D}+\underline{V_S})}{\underline{R_L}}-\frac{\underline{V_M}+\underline{V_D}+\underline{V_S}}{\overline{R}_K}\right]. \quad (3)$$

The right-hand side of (3), which represents the collector current of the ON transistor, consists of two terms. The first term is the negative current flowing from V_{CC}, and the second term is the positive current flowing from V_{BB}.

We wish to evaluate R_B and R_K such that the circuit is operable under an accumulation of worst possible conditions. Although 1 per cent resistors are used throughout the NOR circuit, it is desirable to tolerate an end of life variation of ± 5 per cent. Similarly, we permit long-term power supply variations of ± 5 per cent. Eqs. (2) and (3) further point up the desirability of low diode forward voltage, low transistor saturation voltage and low leakage currents. The maximum permissible values for these parameters are included in the transistor and diode specifications which appear in the appendix. In working with (2) and (3), the most detrimental condition of each parameter is indicated by an underline or overline, designating whether the worst case for the parameter is its minimum or maximum limit respectively. Although no minimum value is specified for either V_D or V_S, the minimum value for their sum is taken as 0.25 volt in the calculations. The minimum value for V_M is 0 volts. Note also that the worst case for (2) is at 55°C where the maximum value of V_D (with a temperature decrement of 2 millivolts per degree C) may be taken as 360 mv.

Suppose that we arbitrarily select a relatively large value for R_K and compute the value of R_B from (2). For every change in R_K, we must make a corresponding change in R_B. From inspection of (3) we note that as we allow R_K to decrease below the point where five full loads can be driven, $MI_{CO}+NI_{DO}$ increases. This increase is desirable because it allows a larger fan-out of the input drivers. A decrease in R_K, however, allows more base current to flow, increases the depth of transistor saturation, and requires a larger coupling capacitor to overcome hole storage effects. Where speed is to be compromised with fan-in and fan-out capabilities, as in this case, it is desirable to use the largest value of R_K compatible with driver fan-out requirements. Where maximum fan-in and fan-out capabilities are desired, the optimum values for R_K and R_B are best determined with computer assistance. The value of R_K selected in this case, *i.e.*, $4.32K$, provides for a maximum $M+N$ value of 22 collectors and diodes. (We have assumed that $\overline{I}_{CO}=\overline{I}_{DO}=40$ microamperes.) This value has proved quite adequate in practical use of the NOR circuits.

Selection of a value for the coupling capacitor, C_K, is based entirely upon the hole storage clean-up requirements of an ON transistor. Measurements on 2N393 transistors indicated that the stored base charge could reasonably be held to 260 micro-microcoulombs at 55°C. The maximum value of stored base charge occurs at maximum base current, maximum collector current, and maximum ambient temperature. The maximum base current is given by

$$I_{B\max}=\frac{\overline{V}_{CC}}{\underline{R_L}+\underline{R_K}}-\frac{\underline{R_L}}{\underline{R_L}+\underline{R_K}}\left(\underline{M}\underline{I}_{CO}+\underline{N}\underline{I}_{DO}\right)-\frac{\underline{V_{BB}}}{\overline{R}_B}, \quad (4)$$

and the maximum collector current is given by

$$I_{C\max}=\frac{\overline{V}_{CC}-(\underline{V_D}+\underline{V_S})}{\underline{R_L}}-\frac{\underline{V_M}+(\underline{V_D}+\underline{V_S})}{\overline{R}_K}. \quad (5)$$

Therefore, under worst conditions, the minimum voltage change impressed across C_K at the diode bus point

given by

$$[C_{K\min} = \overline{V}_{CC}\frac{\underline{R}_K}{\underline{R}_L + \underline{R}_K} - (\underline{M}\underline{I}_{CO} + \underline{N}\underline{I}_{DO})\frac{\underline{R}_L\underline{R}_K}{\underline{R}_L + \underline{R}_K} - (\underline{V}_D + \underline{V}_S), \quad (6)$$

where the position of the underline or overline is determined from (4) and (5).

Since the external stored charge must balance the internal stored charge, we may write

$$(C_K V_C)_{\min} \geq \overline{Q}_S - \frac{\underline{V}_{BB}}{\overline{R}_B} T, \quad (7)$$

where $\overline{Q}_S$ represents the maximum permissible value of stored base charge. The term $(\underline{V}_{BB}/\overline{R}_B)T$ represents the cancellation of stored charge afforded by the reverse current from V_{BB} during the transistion time T. Taking $\underline{M}\underline{I}_{CO} = \underline{N}\underline{I}_{DO} = 0$, $\underline{V}_D + \underline{V}_S = 0.25^V$, and $T = 0.1$ μsec, we may compute C_K as 55 μμf. The nearest 5 per cent value of 56 μμf is used in this case.

The NOR gate was originally intended for a nominal repetition rate of 200 kc. Tests and calculations both verify that 1-mc operation is easily possible, but the auxiliary transfer and one-shot packages to be described below are not recommended for use above 500 kc.

The Dual NOR Package

In many instances a five-input gate is not required. An inverter is one application which requires a single input. A two-input AND function, which is needed quite frequently for gating operations, may be generated quite simply if the inverted variables are available. For example, the function AB is obtained directly from a NOR gate if $\overline{A}$ and $\overline{B}$ are applied at the inputs. In any case, a two-input gate can materially reduce the number of unused diodes in the system. The dual gate structure shown in Fig. 4 provides this facility, and at the same time increases the system packing density.

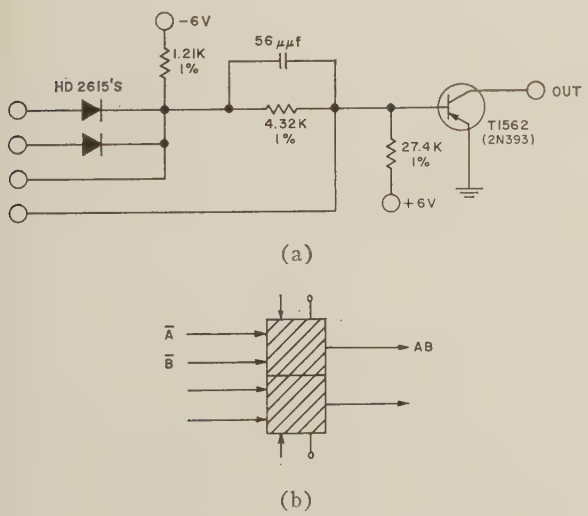


Fig. 4—(a) The dual NOR circuit—two per package—and (b) the dual NOR logic symbol.

The NOR Flip-Flop

Memory, or storage, is necessary to any complete logic scheme. A flip-flop can provide such memory and, in fact, lends itself nicely to the NOR type of circuitry. It is possible to connect the basic NOR circuit as a flip-flop in several ways. The most straightforward method is to interconnect the inputs and outputs of two NOR gates. In this way a dual NOR package could serve as a flip-flop with a single set and single reset input. This type of connection is sketched logically in Fig. 5. Although this type of flip-flop works quite well, it is not recommended as the best possible method of obtaining a flip-flop. A better method, which provides an additional set and reset input, is illustrated in the circuit diagram of Fig. 6(a). In this circuit the transistor collectors are not tied to input diodes, but are connected directly to the diode bus points. Quite fortunately it turns out that the internal diode to which each collector would ordinarily be connected is unnecessary. This occurs because a transistor collector which is connected to a set diode is actually being driven to the ground state when a ground input is received on one of those diodes. Hence the diode isolation is not required. Since the diode bus point is brought out on the NOR and dual NOR packages, a flip-flop can always be constructed as shown in Fig. 6(a). When a dual

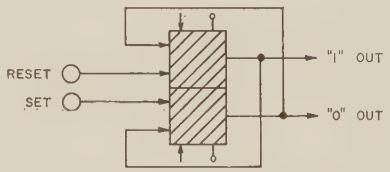


Fig. 5—The dual NOR connected as a set-reset flip-flop.

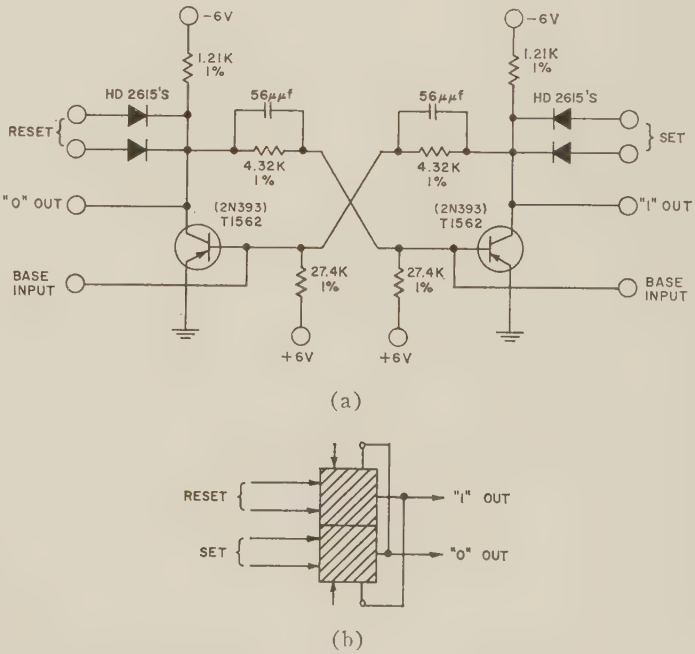


Fig. 6—(a) The NOR flip-flop and (b) the logic symbol used when the dual NOR is so connected.

NOR is connected as a flip-flop, the logic symbol shown in Fig. 6(b) is used. Separate transistor base leads are also brought out on this package, and indicated by the upper and lower vertical arrows in the logic symbol of Fig. 4(b). These inputs are used only in connection with the transfer package which is described below.

It should be noted that the outputs of two or more NOR gates may be paralleled to provide the disjunctive sum of the output functions. In this way the standard OR operation may be obtained by a simple solder joint. In connection with the flip-flop, the ability to parallel outputs provides an additional means of setting and resetting the flip-flop. Fig. 7 illustrates a method which may be useful in some cases. Rather than drive the set or reset terminals directly, the set and reset signals may be applied directly in parallel with the outputs, as shown.

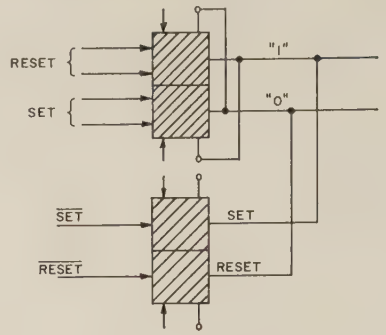


Fig. 7—An alternative method of setting and resetting the flip-flop.

Transfer Package

A transfer package has been designed primarily to simplify the shift register logic problem. Logically speaking, such a package is unnecessary. Its value can only be judged in terms of the convenience and over-all economy which it provides. A schematic of the transfer circuit is shown in Fig. 8(a) and the corresponding logic symbol in Fig. 8(b). The inputs to this circuit are driven by the outputs of a flip-flop whose state is to be transferred to another flip-flop. Fig. 9 illustrates such an application. Let us assume that the upper input to the transfer package is connected to a flip-flop which is in the ONE state. This implies that the upper input is at ground potential, and that the right-most of the two capacitors in the circuit is standing off a voltage approximating 6 volts. The left-hand capacitor, however, will have only a small potential across it, since the lower input will be returned to the ZERO or negative voltage state of the sampled flip-flop. When a ground, or a normal ONE signal, is applied to the transfer input, the charge on the two capacitors is transferred to the output terminals. Since the right-hand capacitor is charged, a positive pulse appears at the upper output terminal. No pulse appears at the lower output since the left-hand capacitor contains practically no charge. If these outputs are now connected to the appropriate base terminals of another flip-flop, that flip-flop will assume the state of the sampled flip-flop. The positive output pulse must, of course, be fed to the base of that transistor which is to be turned off.

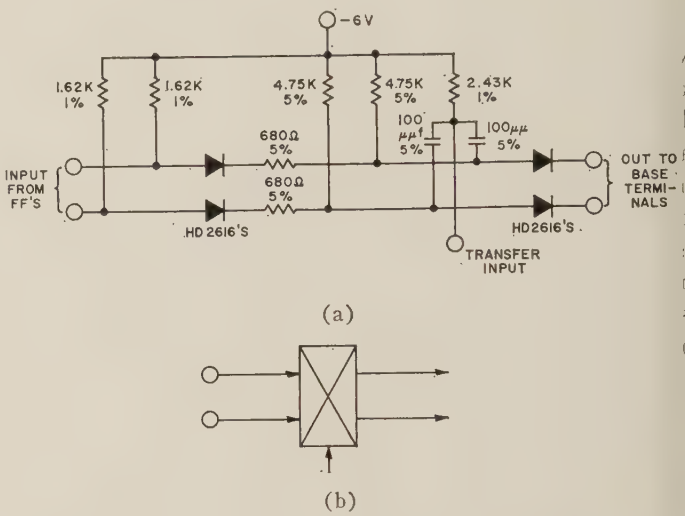


Fig. 8—(a) The transfer circuit and (b) the transfer logic symbol.

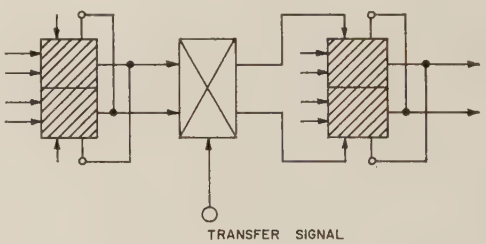


Fig. 9—Use of the transfer package in a shift register.

The diodes in this circuit serve two purposes. The left-hand diodes provide for a unidirectional flow of information. The right-hand diodes isolate the flip-flop bases from the transfer circuitry, and provide an OR gate where two transfer packages drive the same flip-flop. The 680-ohm resistors in series with these diodes assist in preventing charge loss through the left-hand diodes during their reverse recovery time. The 4.75-kilohm resistors provide a recovery path for the capacitors when the state of the sampled flip-flop is altered without the use of transfer circuits. The 1.62-kilohm resistors assure an input voltage from the driving flip-flop of at least 5.25 volts, and minimize the reverse transient effects resulting when the transfer input goes negative.

It might be argued that the addition of one or two diodes directly to a transistor base allows leakage currents to flow which were not considered in the worst-case design of the NOR circuit. This leakage current, however, is present only when a transfer package is driving a flip-flop. The particular connections used in obtaining a flip-flop remove the diode-forward-voltage term from the OFF equation. The loss of this term from (2) more than offsets the leakage currents contributed by two worst-case diodes.

During the transfer process, the state of the driving p-flop is not affected. When the state of the driving p-flop is changed, at least 1.5 μsec must be allowed ior to the initiation of a transfer pulse in order to allow e capacitors within the transfer package to reach equirium. For the same reason, succeeding transfer operaons require removal of the transfer ground for at least 5 μsec.

There is one other application wherein the transfer ckage may be used to significant advantage. In this plication, the standard flip-flop is converted to a mplementing flip-flop. Fig. 10 illustrates this use of e transfer package.

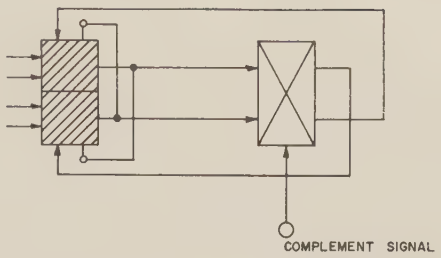
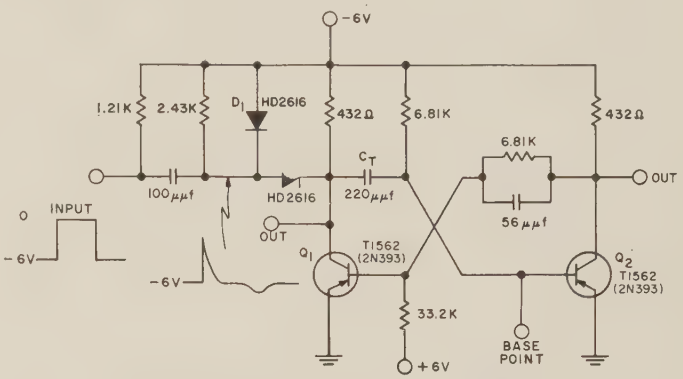


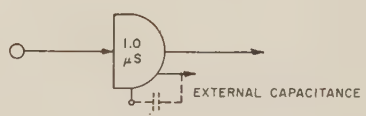
Fig. 10—Use of the transfer package to complement a flip-flop.

The One-Shot Package

No logic system is complete without some means of otaining delay. In the present system a monostable ultivibrator, or one-shot, was selected to provide the lay function. This type of circuit was selected in preference to passive delay lines in order to avoid the mistch and attenuation problems characteristic of these es when the terminating impedances are switched er large ranges. In addition, much longer delays are ossible with one-shots than are readily achieved with lay lines. The circuit used is shown in Fig. 11(a) along ith its logic symbol in Fig. 11(b). In one sense this rcuit is no more than a modified NOR flip-flop. In any se, the operation of a one-shot is sufficiently well nderstood that only a summary of its performance will e given. The circuit is capacitively coupled, and arnged to trigger on positive-going waveforms. The outut is normally at ground, and goes negative for a time ependent upon the value of the coupling capacitance r. Each package is built to provide a pulse duration of ne μsec. Longer periods may be obtained by adding 220 uf of external capacitance for each additional μsec reuired. When the one-shot package is used to obtain a pecified delay, two packages are required. The first dermines the magnitude of the delay, and the second which triggers from the trailing edge of the first) deterines the output pulse width.



(a)



(b)

Fig. 11—(a) The one-shot circuit and (b) the one-shot logic symbol.

Transient Performance

When dealing with transient performance, only three asic circuits need be considered. These are the NOR, ne transfer, and the one-shot. In the case of the active rcuits, *i.e.*, the NOR and the one-shot, transition mes are always less than 0.1 μsec. That is, the time aken for the output to change from the ZERO state to ne ONE state, or vice versa, is always less than 0.1 sec. In addition to the transition time, there is a delay me resulting from the finite recovery capabilities of the iodes. All diodes in the NOR circuits are specified for maximum recovery time of 0.2 μsec. In the worst case, nerefore, a single stage of NOR logic will result in a ombined delay and transition time of 0.3 μsec. The exected, or average, total for these times, however, will be 0.1 μsec. In the case of the transfer package, a logic designer need only keep in mind that a 1.5-μsec period is required for the circuit to recover following a transfer input pulse. With the one-shot circuit, no allowance need be made for diode recovery time. One must, however, allow for recovery of the one-shot itself. This time is always less than one-fifth the output pulse width.

Both the one-shot and transfer circuits are capacitively coupled. Hence, certain restrictions must be imposed on the height, width, and rise time of the input pulse. In both cases, the input pulse must be 0.1 μ sec or greater in width, with a rise time of 0.1 μsec or less. In order to prevent triggering on noise pulses,[7] the one-shot has been provided with a natural threshold such that it will not reliably trigger on pulses less than 4 volts in height. For similar reasons the transfer package requires an input pulse greater than 4.0 volts. Since all circuit transition times are less than 0.1 μsec, and voltage levels never deteriorate below the 4.7-volt level, proper inputs to the transfer and one-shot packages are virtually assured.

[7] The one-shot may be falsely triggered by large noise spikes on the minus 6 volt bus. Where a long lead from the power supply is required, local filtering should be employed to eliminate power supply noise.

Loading Considerations

Problems attendant to loading any particular package have been simplified as much as possible. The load presented by every input is standard with the exception of the transfer input on the transfer package. The load presented by this input is half the standard equivalent load. Therefore, a package which is capable of driving 5 standard loads is capable of driving 10 transfer input loads. The other inputs on the transfer package are standard and represent standard loads. An effort has been made to summarize all of the static loading characteristics in a convenient pictorial form. This summary appears in Fig. 12 and should be self-explanatory.

Transient loading during positive-going transition times, is, of course, always greater than static loading. During this period additional current is drawn by the driving collector in order to discharge coupling capacitors, and stray capacitance to ground. However, the same capacitors which provide hole storage clean-up in the NOR circuit also provide overdrive during the positive-going output transient. If the static loading capabilities of the NOR circuit are not exceeded, sufficient overdrive is always available to permit each collector to drive 100 $\mu\mu$f of stray capacitance, in addition to coupling capacitance, without appreciably increasing the positive-going collector transition time. The negative-going transition may be slightly increased, due to the additional time required to charge the stray capacitance to ground.

Temperature Characteristics

The temperature characteristics of the three basic circuits cannot be discussed apart from considerations of loading. The loading capabilities of each package were determined on the basis of worst possible conditions. With respect to temperature, this meant +55°C. Accordingly, maximum diode and transistor leakage currents are specified at this temperature. Worst-case temperature specifications on diode forward voltage and collector saturation voltage, however, are not as clear-cut. Diode forward voltage decreases with temperature at a nearly linear rate. For germanium, this rate is about 2.3 mv per degree C. Since diode forward voltage is specified at 25°C, some margin is obtained at the higher temperatures by computing the voltage decrement at only 2 mv per degree C. In the case of collector saturation voltage, two processes conflict in the determination of the rate and sign of the temperature variation. Theory predicts a linear increase in voltage due to a temperature increase alone. Increasing temperature, however, also affects the current gain of the transistor. Although the latter effect is small, it results in a logarithmic change in saturation voltage. The actual sign of the temperature variation, therefore, is in doubt. Fortunately, the total change is itself small, and partially masked by voltage drops in the collector and emitter series body resistances. Because the resultant

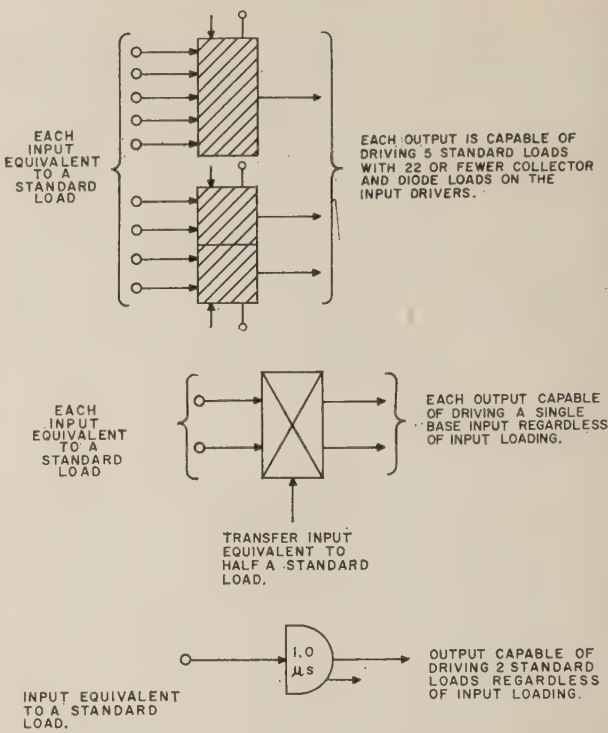


Fig. 12—Summary of loading characteristics.

change is almost negligible, collector saturation voltage is specified at 55°C where the greatest difficulty is encountered in meeting other performance standards.

The stored base charge of a saturated transistor is another parameter which is quite sensitive to temperature. Measurements have shown that the quantity of charge stored may increase by as much as 20 per cent as the temperature is raised from 25° to 55°C. Accordingly, the transistor hole storage specification is also made at 55°C.

Package Design

No effort will be made here to justify the physical package design ultimately selected to house the individual circuits. It is sufficient to note that considerable effort was expended in that direction, and a suitable selection made. Photographs of the four individual plug-in elements are shown in Figs. 13–16.

Operating Experience

Over a period of 11 months, approximately 3000 of the basic logic packages have been placed in operation. In addition, over 400 special package types to handle input-output equipment, core and drum memories, etc. have been used. Of the 3000 standard types, approximately 60 per cent are dual NORs, 18 per cent are single NORs, 12 per cent are transfer elements, and 10 per cent are one-shot elements. During this time, over 2,000,000 transistor hours have accumulated, all during prototype construction and check-out. Component failures during this period ran as follows: 55 transistor failures, 5 diode failures, 3 resistor failures, and 1 connector failure. The number of transistor failures may

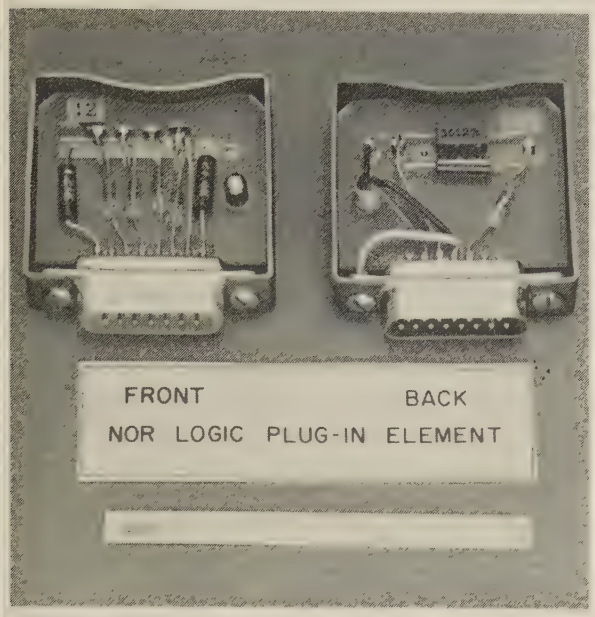


Fig. 13—Front and back view of the NOR package.

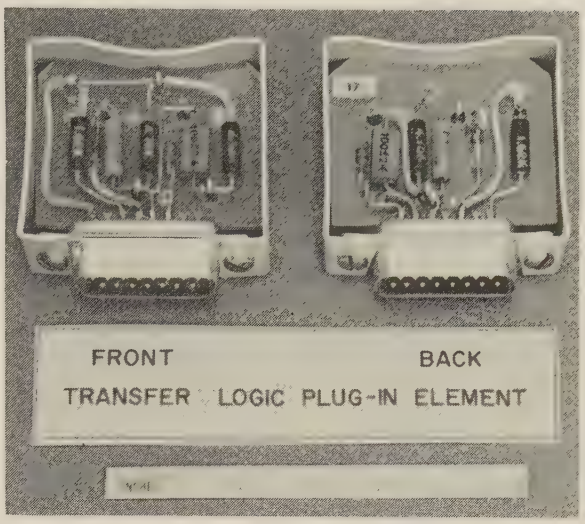


Fig. 15—Front and back view of the transfer package.

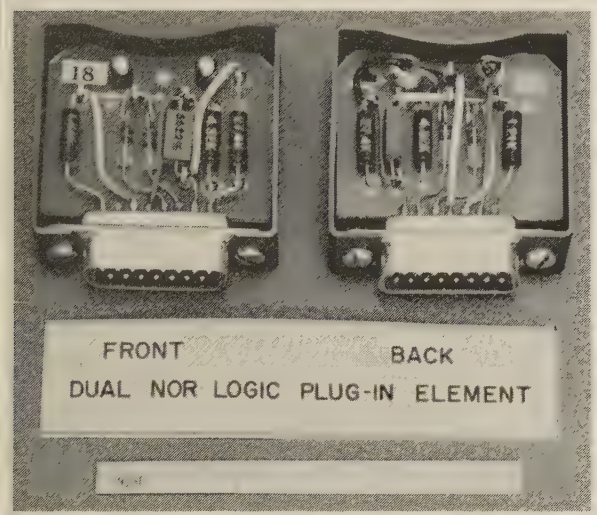


Fig. 14—Front and back view of the dual NOR package.

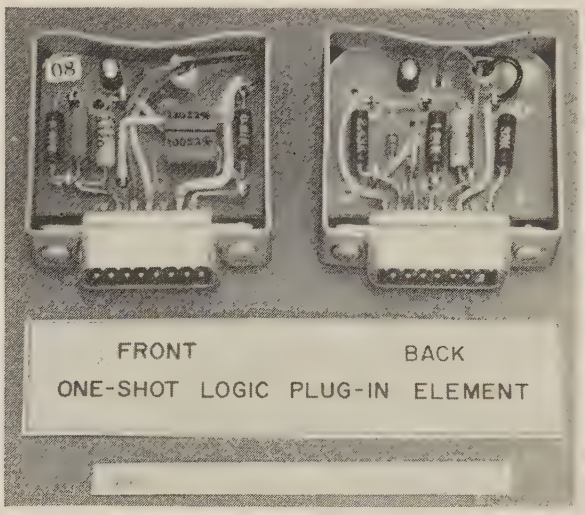


Fig. 16—Front and back view of the one-shot package.

pear excessive. However, the majority of these can attributed to "screwdriver" errors where the transis- was mistreated during system check-out. The exact mber of transistors which failed without human inter- ntion is unknown, but presumed to be of the order of or 6. Similar remarks apply to the number of diode lures where human intervention is estimated to have luced perhaps 3 of the 5 failures.

Conclusion

A unique set of compatible logic packages has been scribed. This set is unique in the sense that a single pe of diode-transistor circuit is used to provide the eat majority of logic and storage functions required the system.

Experience has shown that this logic set is quite flexi- . In common with the direct-coupled transistor mode operation, it permits paralleling of transistor collectors to provide the OR function. In addition, the present system of logic provides considerable economy over those types, such as DCTL, which use a transistor base for every logic input. Furthermore, the capacitive coupling employed permits the transistor to operate near its maximum capabilities. Although no effort was made to achieve high speed of operation in the present logic system, it is believed that the selection of higher speed diodes, in conjunction with a few minor circuit alterations, would enable the diode NOR circuits to operate with stage delays of 100 mμsec or less.

Appendix

Diode and Transistor Specification

Specifications are given for the logic diode and the microalloy transistor. Two types of diodes are employed, differing from one another only in their recovery time.[8]

[8] HD 2616 Diode has a 0.3 μsec recovery requirement.

Germanium Diode—HD 2615

Forward V	$\leq$420 mv @ +25°C and 5 ma
Reverse V	$\geq$30v
Reverse I	$\leq$40 μa @ +55°C and 6v
Reverse I	$\leq$10 μa @ +25°C and 10v
Recovery to 30 k from 5 ma fwd to 6^V reverse	$\leq$0.2 μsec
Continuous dc forward current	100 ma Maximum Rating at +25°C
Surge current for 1 second	500 ma Maximum Rating at +25°C
Average power dissipation	80 mw Maximum Rating at +25°C
Derating above 25°C	10 mw/10°C

Germanium Micro Alloy Transistor—T 1562

Absolute Maximum Ratings:

Storage temperature	85°C
Junction temperature	85°C
Collector voltage V_{CB}	10v
Collector voltage V_{CE}	8v
Collector current	50 ma
Total device dissipation at 55°C	25 mw
Lead temperature @ $1/16'' \pm 1/32''$ from case	230$\pm$5°C for 10 seconds

Electrical Characteristics:

Collector cutoff current (I_{CBO} @ 8v)	$\leq$40 μa @ 55°C
Emitter cutoff current (I_{EBO} @ 2v)	$\leq$20 μa @ 55°C
On condition (I=25 ma, I=0.625 ma) V_{CE}	$\leq$0.200v @ 55°C
Extrinsic base resistance collector capacitance product, $r_b'C_c$	$\leq$750 $\mu\mu$sec
Maximum frequency of oscillation	$\geq$40 mc
Output capacitance, C_{ob}	$\leq$6 $\mu\mu$f
Hole storage	Fig. 17

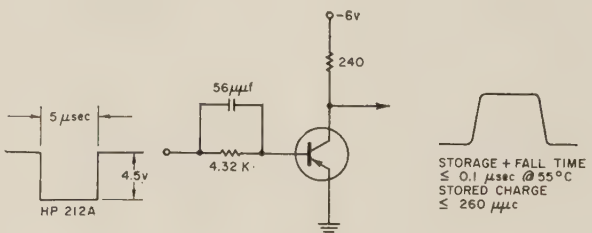


Fig. 17—Hole storage specification.

ACKNOWLEDGMENT

Contributions from members of the Computer Techniques Laboratory, Stanford Research Institute, are gratefully acknowledged.

Esaki Diode High-Speed Logical Circuits*

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Summary—Logical circuits using Esaki diodes, and which are sed on a principle similar to parametron (subharmonic oscillator ment) circuits, are described. Two diodes are used in series to m a basic element called a twin, and a binary digit is represented the polarity of the potential induced at the middle point of the n, which is controlled by the majority of input signals applied to middle point. Unilateral transmission of information in circuits nsisting of cascaded twins is achieved by dividing the twins into ee groups and by energizing each group one after another in a lic manner.

Experimental results with the clock frequency as high as 30 mc e reported. Also, a delay-line dynamic memory and a nondestruc- e memory in matrix form are discussed.

Introduction

ESAKI DIODES, which are also known as tunnel diodes, are highly suitable elements for logical circuits in view of their extremely high frequency nit, compactness, high stability, and low power con- mption. Moreover, the cost can be expected to be very w for mass production quantities in the near future.

An Esaki diode is a two-terminal negative resistance ement which is essentially bilateral. Therefore, unlike rdinary transistor switching circuits, Esaki diode cir- uits require that some special method be incorporated obtain a unilateral characteristic for the transmission nd amplification of digital signals. This situation is mpletely analogous to that which has been en- ountered in the case of the parametron.

To illustrate the application of Esaki diodes to logical rcuits, a system closely related to the logical prin- ples of parametrons will be discussed in this paper. his system of circuitry for Esaki diodes, based on a roposal by E. Goto, has been developed at the Uni- ersity of Tokyo with the cooperation of the Takahasi aboratory of the Physics Department, the Amemiya aboratory of the Applied Physics Department, and the Ioto-oka Laboratory of the Electrical Engineering De- artment. An experimental model whose clock fre- uency is as high as 30 mc has been successfully built.

The Basic Principle

A typical voltage-current characteristic of an Esaki iode is illustrated in Fig. 1. It clearly shows the nega- ve resistance region between A and B which is the

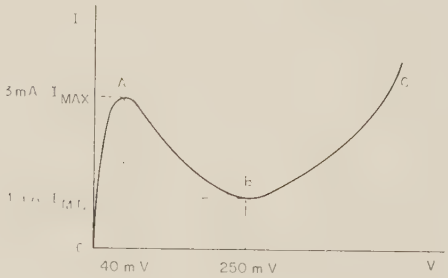

Fig. 1—A typical characteristic of a silicon Esaki diode.

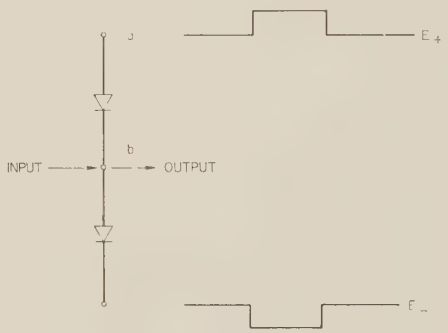

Fig. 2—Basic circuit named "twin."

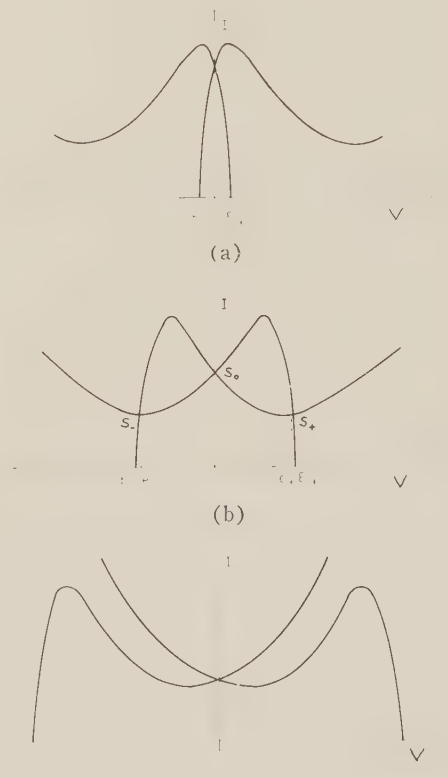

Fig. 3—Response curves of a twin.

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characteristic feature of Esaki diodes. Two Esaki diodes which have almost the same characteristic are connected in series to form the basic circuit shown in Fig. 2, which will be called a "twin circuit" or more simply a "twin." Symmetric exciting voltages E_+ and E_- of equal magnitude and of opposite polarity are applied between a and c. Depending on the magnitude of these exciting voltages, the twin shows three different kinds of response. When the voltages are small, the operating point of each diode, as illustrated by the two curves shown in Fig. 3(a), lies between O and A on the characteristic curve of Fig. 1. Hence, the potential at the middle point b is zero. Similarly, when the voltages are very large, the operating point of each diode of the twin circuit lies between B and C of the characteristic curve (Fig. 1) and the potential of the middle point b is also zero as shown in Fig. 3(c). When the voltages are chosen so that the operating points of both of the diodes of the twin lie between A and B as shown in Fig. 3(b), there are three possible operating points, S_0, S_+, and S_-. The operating point S_0 corresponds to zero potential at the middle point b, and it is unstable because both diodes are in the negative resistance region. Hence, the operating point of the twin diodes will go to either one of the two stable points, namely, S_+ or S_-, which indicates two possible potentials e_+ and e_- at the middle point b of the twin. These two potentials e_+ and e_- have equal magnitude but opposite polarity. A binary digit can be represented by these two potentials in a twin circuit.

When the exciting voltages are switched from a small value corresponding to the case shown in Fig. 3(a) to a value corresponding to the case in Fig. 3(b), the state S_0 having zero potential at the middle point of the twin will become unstable. The potential must flip to either of the two stable values e_+ or e_- [Fig. 3(b)], and these two should be equally probable for a twin consisting of well matched diodes. Under these circumstances, a very small signal applied at the middle point b will be sufficient to control the choice between the two possible states mentioned above. When the square waves shown in Fig. 4(a) are impressed on the twin as exciting voltages E_+ and E_- together with a small control signal $\pm E_n$, the two permissible voltages e_+ and e_- will build up as shown in Fig. 4(b). This process may be regarded as the amplification of the small input signals $\pm E_n$.

Intercoupling the middle points of the twins with each other by means of coupling resistors, logical operations and the transmission of information will be performed in just the same manner as has been done in parametron (subharmonic oscillator) circuits. Unilateral transmission of information will be accomplished by dividing the twins into three groups, I, II, and III, and exciting each group with one of the exciting signals, $E_{I\pm}$, $E_{II\pm}$, and $E_{III\pm}$, which are switched on and off one after another in a cyclic manner as shown in Fig. 5. The direction of information flow will be from group I to II, II to III, and III to I.

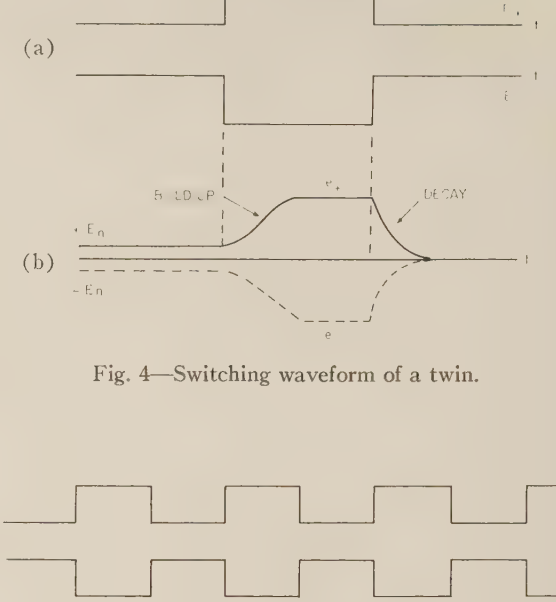


Fig. 4—Switching waveform of a twin.

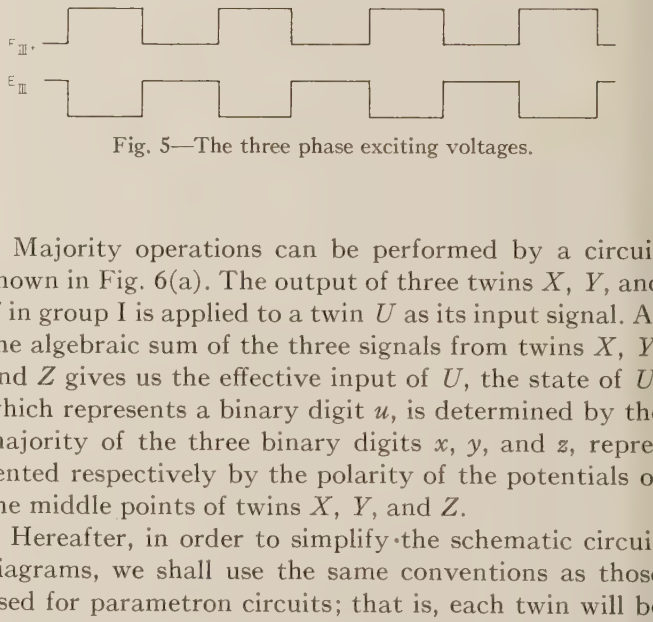
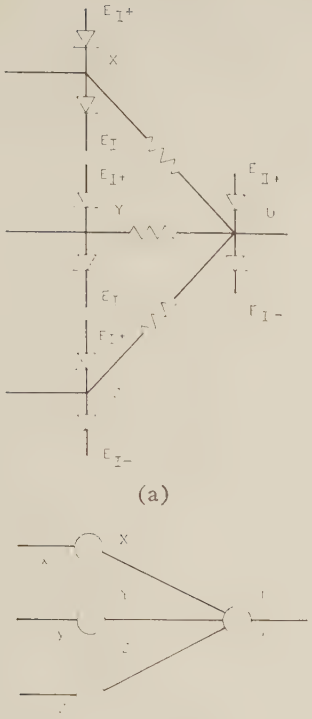


Fig. 5—The three phase exciting voltages.

Majority operations can be performed by a circuit shown in Fig. 6(a). The output of three twins X, Y, and Z in group I is applied to a twin U as its input signal. As the algebraic sum of the three signals from twins X, Y and Z gives us the effective input of U, the state of U which represents a binary digit u, is determined by the majority of the three binary digits x, y, and z, represented respectively by the polarity of the potentials of the middle points of twins X, Y, and Z.

Hereafter, in order to simplify the schematic circuit diagrams, we shall use the same conventions as those used for parametron circuits; that is, each twin will be represented by a small circle. Each pair of circles will be connected by a line when corresponding twins are coupled, one line being used per unit coupling intensity. In each circle representing a twin, the input coupling lines will come into the left side of the circle and the output will go out from the right side of the circle. Instead of showing the existing voltages explicitly, Roman numerals I, II and III will be written above the circles to indicate the kind of exciting voltages (cf. Fig. 5) being used.

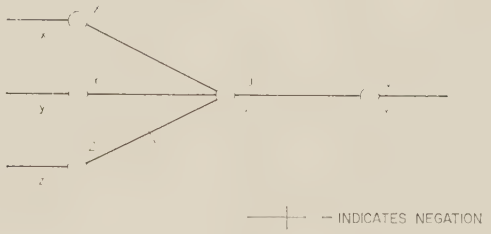
AND and OR operations can be regarded as special cases of the majority operation with a constant bias. A symbol + will be inscribed in the circle representing a twin to indicate a constant input of unit intensity cor-



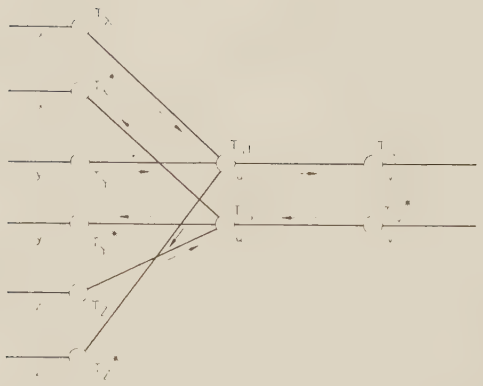
(a)

(b)

Fig. 6—The majority logic.



(a)



(b)

Fig. 7—(a) A majority operation with negation. (b) Negation in symmetric circuitry.

sponding to a binary digit "1," and a symbol − will inscribed to indicate a constant input of unit insity corresponding to a binary digit "0." Accordingly, a circle with + having two input lines represents OR circuit and a circle with −, an AND circuit. Using these conventions the schematic diagram of the circuit of Fig. 6(a) is shown in Fig. 6(b).

Negation or the NOT operation is another basic operation indespensable for general purpose logical circuits. In the Esaki diode twin circuits, however, we shall encounter some difficulties in making a NOT circuit. A NOT circuit changes a binary digit "1" into "0" and "0" into "1," and this means the reversal of polarity of dc signals in the Esaki diode twin circuits. In parametron circuits, since the signals are pure alternating currents, the reversal of the polarity is made simply by means of phase reversing transformers. In twin circuitry, since the signals are direct currents, obviously, transformers cannot be used for the reversal of their polarity. Of course, vacuum tube or transistor amplifiers can be used for reversing the polarity. These amplifiers, however, will cause serious signal delay, which makes these amplifiers unfavorable for extremely high speed operation.

In the twin or Esaki diode circuitry, it is possible to make the NOT operation without a delay by employing a rather elaborate system which may be termed the symmetric or push-pull system. In this system, a pair of two twins are used in a push-pull manner so that when one twin in a pair is holding a certain binary variable x, the other twin in the pair holds the complement $\bar{x}$. For example, the logical circuit shown in Fig. 7(a) is a circuit for making the majority u of three variables x, y, and (not z), and for transmitting u to the next stage v. This logical operation will be carried out by the circuit shown in Fig. 7(b), in which the pairs of twins representing binary variables x, y, z, u, and v are denoted by T_X, T_X^*; T_Y, T_Y^*; T_Z, T_Z^*; T_U, T_U^* and T_V, T_V^*. It can be seen from the figure that by setting up the symmetric configuration once at the input, the entire circuitry of a machine can be constructed in the push-pull configuration. Calling the twin in a pair with no asterisk the front (push) twin, and the other (with asterisk) the back (pull) twin, a coupling line without negation in the logical diagram [Fig. 7(a)] may be interpreted to require coupling between corresponding front twins and between corresponding back twins. A coupling line with negation may be interpreted as the cross coupling between the corresponding front twins and the opposite back twins.

The increase of number of elements is obviously a disadvantage of this symmetric system. On the other hand, besides the speeding up of negation, there are two other interesting advantages of the symmetric system. One is its single significant error detecting property. An erroneous operation in either T_Z or T_Z^* in Fig. 7(b) will be called significant if $x=\bar{y}$ and $\bar{x}=y$ hold. The presence of an error in this case will be detected by the fact that $v=\bar{v}$ at the twins T_V and T_V^* in the last stage. On the other hand, if $x=y$ and $\bar{x}=\bar{y}$, the final result will be $v=x=y$ and $\bar{v}=\bar{x}=\bar{y}$ independently of z and $\bar{z}$. Hence, an erroneous operation of twins T_Z and T_Z^* will not have any significance in the result of the computation. Suppose we have a large scale computer made entirely of

this symmetric scheme. Then, an erroneous operation of a twin in the accumulator will be significant if it occurred just before printing out of the accumulator content, and it will not be significant if it occurred just before the content is reset to zero. Therefore, it will be possible to detect significant errors by providing a relatively small number of comparators at the output stage of a large scale computer.

The other advantage is that the signal currents will be balanced perfectly in the symmetric system as shown in Fig. 7(b). In very high speed computers, spurious signals induced by common ground currents would be a very serious problem. By placing the twins in each pair closely together in the symmetric system, the ground currents will be balanced out, and the undesirable effects of ground currents can be completely eliminated.

Experimental Results

An experimental model of a binary counter using the symmetric system has been successfully built. The logical diagram of the circuit is shown in Fig. 8(a), and the complete circuit in Fig. 8(b). In Fig. 8(a), 1, 2, and 3 form a flip-flop circuit to absorb the undesirable effects of chattering in the input switch. 4, 5, and 6 form a so-called digital differential circuit and a single pulse is obtained at 6 each time the state of the flip-flop changes from "0" to "1." 7, 8, 9, and 10 form a binary counter. Therefore, each time the input switch is switched from $-$ to $+$ the binary counter changes its state.

In Fig. 8(b), the input is connected to an asymmetric circuit and it is connected into a symmetric form between 1 and 2* and between 4 and 5* by NOT circuits. For the NOT circuit, both transistor amplifiers and transformer circuit shown in Fig. 9 were tested and both operated successfully. In Fig. 9, as the input to the twin in group II is only one, the transformer without dc restration can be used for negation. However, in this case the negation is accompanied by one stage of delay.

The equivalent circuit of an Esaki diode is shown in Fig. 10. The resistance with an arrow represents the dc characteristic shown in Fig. 1; C is the parallel capacitance, and R_s is the series resistance. The maximum switching speed will be determined by the time constant $\tau = C|-r|$, where $|-r|$ is the minimum of the absolute magnitude of the negative resistance.

Using silicon Esaki diodes made by the Sony Corporation, Tokyo, of which the specifications are $I_{max} = 3$ ma, $|-r| = 100$ ohm, $C = 400$ pf, $\tau = 4.10^{-8}$ second, and using coupling resistors of 2000 ohm, the binary counter circuit of Fig. 8(b) has been operated at 1 mc. Similarly, using germanium Esaki diodes (made by the Sony Corporation) of which the specifications are $I_{max} = 3$ ma, $|-r| = 10$ ohm, $C = 40$ pf, $\tau = 4.10^{-10}$ second, and using coupling resistors of 500 ohms, the same counter circuit has been operated successfully at the clock frequency of 30 mc. The frequency was limited to 30 mc because of the characteristic of the oscilloscopes presently available at the University of Tokyo. By comparing the time constants τ of both diodes, it seems possible to obtain a clock frequency as high as 100 mc with the present germanium Esaki diodes.

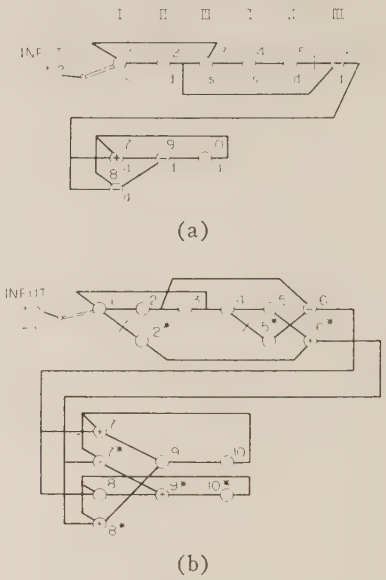


Fig. 8—(a) A binary counter with logical input. s indicates asymmetric circuits. d indicates symmetric circuits. (b) Full circuit diagram of Fig. 8(a).

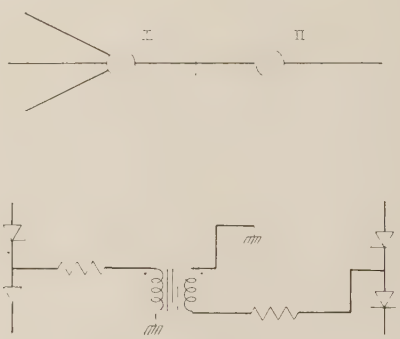


Fig. 9—NOT circuit by transformer.

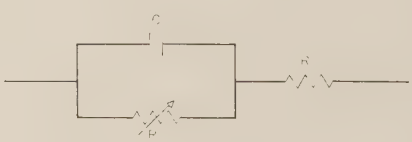


Fig. 10—Equivalent circuit of Esaki diode.

In these experiments the value of the coupling resistances have been determined so as to ensure a logical gain (the maximum number of inputs+outputs) of 10. From these experiments one may observe the fact that the relation between clock frequency f of the twin circuitry and the time constant should be given approximately by $f \cdot \tau \simeq 8$ to 25. This fact implies that the future development of better Esaki diodes having time constants of less than $4 \cdot 10^{-11}$ second would result in a billion bit rate (1000-mc clock) machine.

Exciting power supply circuits used in the experiments are shown in Fig. 11. Instead of the square wave shown in Fig. 5, a superposition of dc biasing voltage

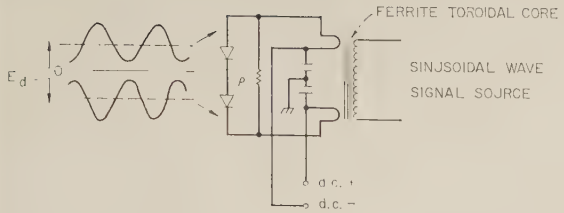


Fig. 11—Exciting voltage supply circuit

nd pure sinusoidal voltages is used. The resistor ρ(20 hms) is used for reducing the source impedance, and ost of the source power (about 1 mw per twin circuit) consumed by this resistor.

One of the important facts in the Esaki diode twin cir-uitry is the balance between the diodes. The maximum ain and stability depends critically on the balance. It found that balancing I_{max} of the diodes is most criti-al. In our experiment, I_{max} in a twin was matched ithin ± 3 per cent tolerance to insure the operation of he counter [Fig. 8(b)] consisting of seventeen twins. he dependence of the balance on the parameters of iodes has been investigated by using the parametron igital computer (PC-1) which simulates the Esaki iode circuitry. The results will be published in the ear future.

Memory Circuits

Two kinds of memory devices using Esaki diodes ave been tested. The one is a serial delay-line memory roposed by E. Goto. The circuitry of this memory is own in Fig. 12. A coaxial delay line cable with an open eflecting end is connected to the middle point of a win. The state of the twin is controlled by the reflected gnals, and a circulating dynamic memory circuit is rmed. A 16-bit memory circuit at a 30-mc clock fre-uency using standard coaxial cables (75-ohm im-edance, 5-mm diameter, and polyethylene filled) has een operated successfully. This delay line memory ill be suitable for serial type computers.

The other is a nondestructive readout matrix array f diode twins proposed by K. Murata. Fig. 13 shows he basic circuit for each binary digit which is inserted t the cross point of an X-Y matrix array. In the normal tate, dc holding signals (of value corresponding to Fig. (b)) are applied to A_+ and A_-. The nondestructive eadout is made by varying the voltage of one of the X nes A_+ and A_- and by sensing the polarity of varia-ion of the current in the Y line or lines. A double coin-idence writing is effected by varying the voltage of A_+ nd A_- of an X line to facilitate the change of the state

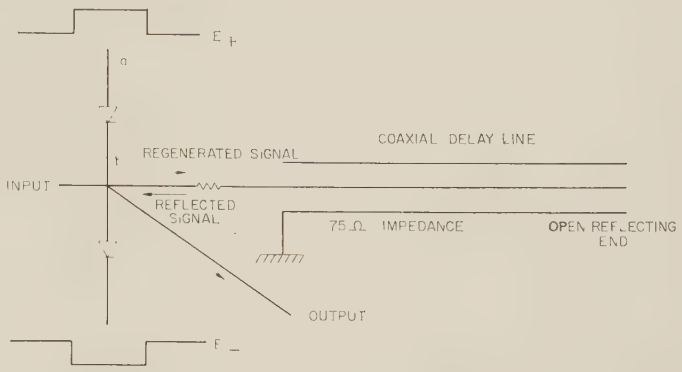


Fig. 12—Delay-line regenerating memory.

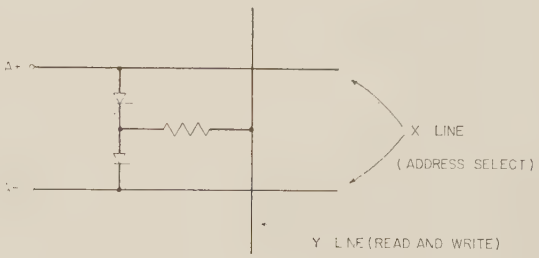


Fig. 13—A twin diode memory cell.

and by applying a writing voltage to a Y line. The results of tests made on a single basic unit are very promising. However, the number of Esaki diodes available at the present has been insufficient to build a full scale experimental matrix.

Acknowledgment

The authors wish to express their sincere gratitude to M. Ibuka (President), and Dr. L. Esaki of the Sony Corporation, Tokyo, for much useful information, and for supplying diodes without which it would have been impossible to accomplish the experiments. Gratitude is also extended to Professor H. Takahashi of the Department of Physics and to Professor A. Amamiya of the Department of Applied Physics of the University of Tokyo for helpful discussions and encouragement.

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Magnetic Analogs of Relay Contact Networks for Logic*

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Summary—Two techniques are described for designing multi-apertured magnetic structures capable of realizing any specific logic function. The structures are made from rectangular hysteresis loop material. The designs are derived from the corresponding relay contact network by replacing each current carrying conductor in the relay circuit with its analog in the magnetic circuit, a flux-carrying conductor, replacing the emf with a pulsed mmf; and replacing each back contact with a saturable portion of the magnetic circuit in the topological equivalent of the contact network. A flux reversal through a saturated portion may then be blocked by means of an inhibiting current applied to a suitable winding, the current representing a logical input variable. Thus flux may be "steered" through the magnetic circuit in a manner analogous to the steering of current through the contact network. For planar structures the first technique may be used to obtain the analog of series-parallel and bridge type circuits; the second technique is suitable only for the analogs of series-parallel circuits. It is pointed out that the analog of a relay tree can be used as a standard structure suitable for realizing any Boolean function. Representative examples of both designs are shown, and experimental data are given.

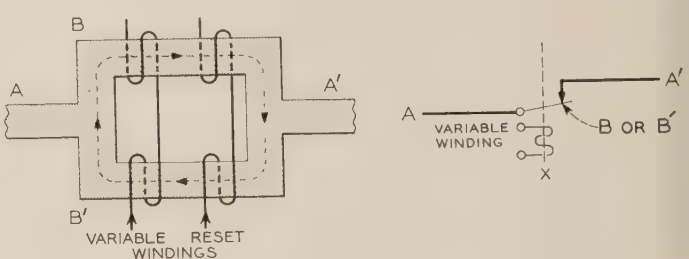
I. Introduction

During the past several years a number of multi-aperture magnetic devices made from rectangular hysteresis loop material have been developed for use as logic elements.[1–4] These devices have attractive features, such as low cost and low power requirements, and suggest the likelihood that other magnetic structures might be even better in some applications. In this paper we consider two related, but different, techniques for arriving at magnetic structures capable of realizing specific logic functions. In addition, it is pointed out that these techniques can be used to obtain standard structures which will realize any logical function (with the size of the structure imposing limitations as to the maximum number of variables, of course).

Both of the techniques to be described here start by considering a planar contact network which realizes the desired logical function. More or less straightforward rules can then be given for obtaining the magnetic analog of this circuit. Thus, it is possible to apply well-known techniques developed for relay contact networks in order to obtain certain advantages in the magnetic analog, *e.g.*, a reduction in the number of windings required. After a brief discussion of each method, a short comparison is made of the devices obtained in this manner with one another and with the equivalent laddic circuitry.

II. First Method

The first method of realizing relay-like logic with magnetic circuits follows upon recognizing that the device of Fig. 1(a) is the magnetic analog of a relay back contact, shown in Fig. 1(b). The shaded region in Fig. 1(a) is square loop ferrite material, consisting of series arms A, A', and the magnetic loop structure BB'. The cross-sectional areas of arms A, A' and the side-arms of BB' are equal. Loop BB' carries a reset winding and a variable or "hold" winding as shown.



(a) (b)

Fig. 1—A relay back contact and its magnetic circuit analog.

A current pulse, applied to the reset winding sets up a saturated flux loop in the direction of the arrows shown in Fig. 1(a). In order to satisfy the condition of flux continuity the arms A, A' will be magnetically neutral following reset. If an external magnetomotive force is now applied to AA', a flux reversal will take place either through $AB'A'$ or $A'BA$ depending on the polarity of the applied mmf. However, if at the same time a hold current representing a variable x is applied to the variable winding to maintain flux saturation in loop BB', the flux reversal is inhibited.

Note that flux can be switched, when not inhibited by a hold current, no matter whether the external mmf acts from A towards A', or from A' towards A, since the flux in side arm B can be reversed in one direction, and the flux in side arm B' in the opposite direction. Thus, the

* Manuscript received by PGEC, September 23, 1959; revised manuscript received, December 28, 1959.

† Bell Telephone Labs., Inc., Murray Hill, N. J.

[1] U. F. Gianola and T. H. Crowley, "The laddic—a magnetic device for performing logic," *Bell Sys. Tech. J.*, vol. 38, pp. 45–72; January, 1959.

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[3] N. F. Lockhart, "Logic by ordered flux changes in multipath ferrite cores," 1958 IRE National Convention Record, pt. 4, pp. 268–278.

[4] H. D. Crane, "A high-speed logic system using magnetic elements and connecting wire only," Proc. IRE, vol. 47, pp. 63–73; January, 1958.

ructure is bilateral, as must be the case if it is to be a ue analog of the relay circuit shown in Fig. 1(b).

The analogy to operation of a relay back contact is vident. In the latter, a current representing the varia- le x energizes the relay coil [Fig. 1(b)] and opens con- act B, thus preventing an external source from driving urrent through the series path ABA' in either direction.

It will now be apparent that a magnetic circuit can be uilt which is the direct analog of any planar relay cir- uit employing back contacts; one merely substitutes a aturable magnetic loop BB' for every back contact and magnetic series arm for every conductor in the relay ircuit. If sources are available for each variable and its egation, then the analog of any planar circuit can be btained. If sources are available only for each variable or for the negation of each variable), the analog of he so-called "frontal" function[5] can be obtained. In ddition, it is now a simple matter to design the mag- etic analog of any bridge circuit. Since bridge circuits requently realize a given logical function with less con- acts than does a series-parallel circuit, use of this tech- ique may result in fewer variable windings than can be btained using magnetic structures which realize series- arallel circuits, *e.g.*, laddics.

Usually the variable and reset windings in Fig. 1(a) an be simplified, because in all branches of series-paral- el networks, and in most of the branches of bridge net- orks, unidirectional conduction only is required. In hese cases the two windings need not link both side- rms. For example, if the external magnetomotive force s applied in the direction A to A' in Fig. 1(a), the ariable and reset windings need link only the lower side- rm, B' of the loop.

To put the above principle to test, the magnetic quivalent of the common bridge circuit, shown in Fig. (a), was fabricated and tested. The geometry of the nagnetic bridge might be as illustrated in Fig. 2(b). The eset winding is not shown, but would consist of a single inding, linking all five magnetic loops in series. The ariable, drive, and output windings are indicated, as ell as the reset flux pattern.

The operation of this circuit is as follows: A clock rive D attempts to switch flux in branch 1 in the direc- ion indicated. If all paths through the bridge are locked, then the drive will switch flux clockwise around he outer path consisting of branches 1 and 2. However, f a path is available through the network the drive will witch flux through it, and not through branch 2, if the atter is appreciably longer than the longest path hrough the bridge. This by-pass principle is the same s used in laddics.[1]

It is evident that winding f_a yields the "hindrance" unction of the bridge network, while f_b yields its com- lement, the "transmission" function. Specifically,

$$f_a = x_1x_2 + x_3x_4 + x_1x_5x_3 + x_2x_5x_4.$$

[5] E. N. Gilbert, "Lattice theoretic properties of frontal switching unctions," *J. Math. and Phys.*, vol. 33, pp. 57–67; April, 1954.

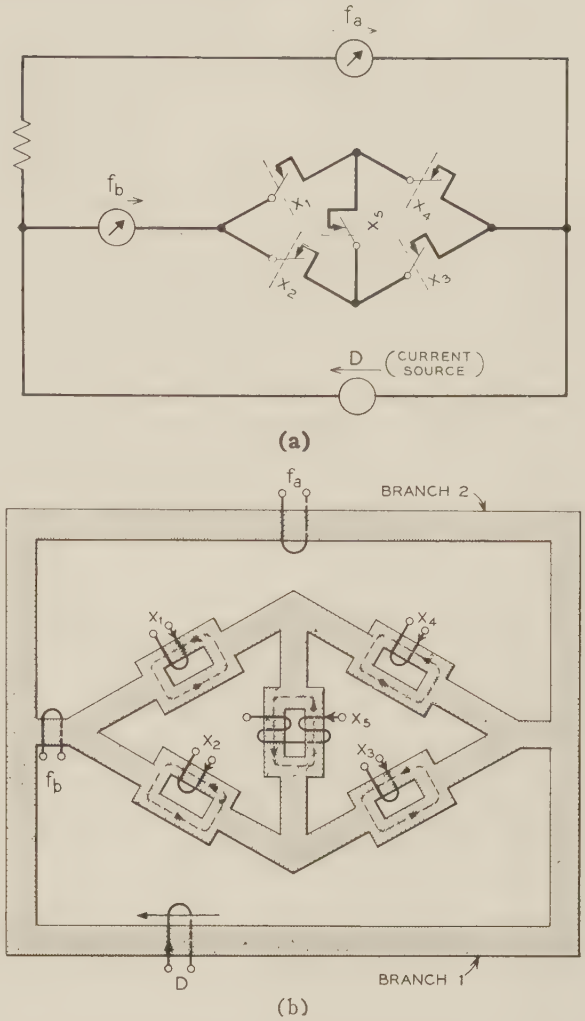


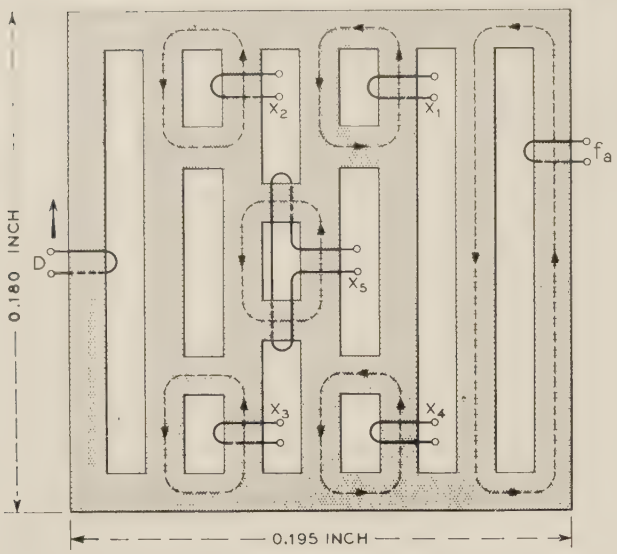
Fig. 2—A relay bridge circuit and its magnetic analog.

It is seen from Fig. 2(b) that only 5 variable windings are required to realize the above function.

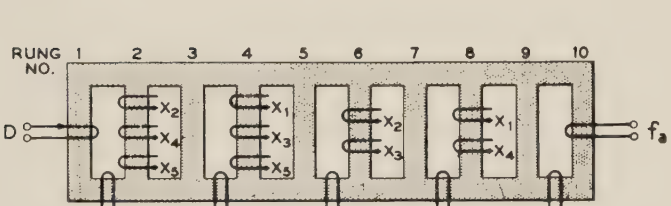
The function can also be written in the form

$$f_a = (x_2 + x_4 + x_5)(x_1 + x_3 + x_5)(x_2 + x_3)(x_1 + x_4).$$

The laddic circuit for realizing this function is shown in Fig. 3(b). A detailed explanation of the operation of circuits similar to this can be found in the article by Gianola and Crowley.[1] For convenience, we include the following brief explanation. A reset winding, not shown on the figure, establishes a flux pattern which consists of loops saturated (in a clockwise direction) in legs 1–2, 3–4, 5–6, 7–8, and 9–10. A clock pulse applied to the winding on rung 1 attempts to switch flux in a counter-clockwise direction. This flux will switch through rung 2, thus inducing no voltage in the output winding, unless there is a pulse at the same time in the winding corresponding to X_2 or X_4 or X_5. If at least one of these pulses is present, the flux will return through rungs 4, 6, 8, or 10. The flux cannot return through the odd-numbered rungs since they are already saturated in the upward direction. In order to prevent flux switching through rung 4, X_1, X_3, or X_5 must be present. Similar statements are true for rungs 6 and 8. Flux is switched



(a)



(b)

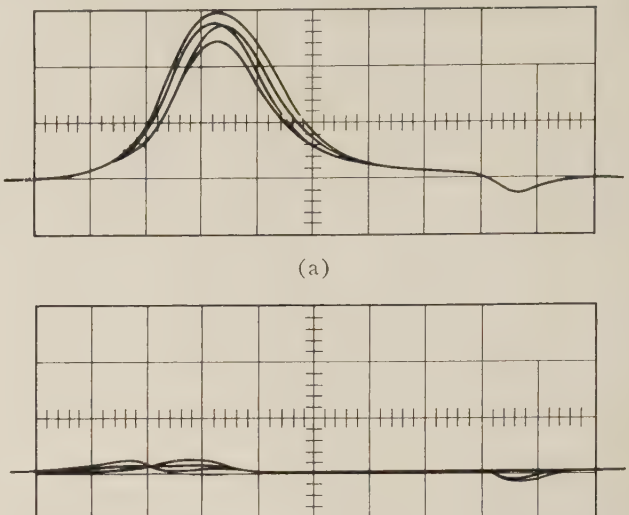
Fig. 3—(a) Geometry of the bridge circuit fabricated for test purposes. (b) Laddic equivalent of bridge circuit.

through rung 10, thus giving an output pulse, if and only if the variables are such that the function f_a is equal to one.

Since the laddic circuit requires 10 windings, the bridge circuit is seen to require 5 less windings.

In fabricating the bridge circuit of Fig. 2, the geometry was modified in order to minimize the length of the connecting arms between magnetic loops. Fig. 3 shows the geometry actually employed and also the variable, drive, and output windings, and the reset flux pattern. The reset winding is again omitted. The reader may observe that the bridge topology in Fig. 3 is not exactly the same as in Fig. 2(b). However, the operation of the circuit is not affected, the modified topology being derived by combining common flux paths where possible to reduce the overall size of the structure. Furthermore, an additional rung has been added to provide a closed flux return for the output rung when reset. This is not essential but helps to improve the signal-to-noise ratio. The dimensions of the experimental structure are shown to scale in Fig. 3.

Photographs of the output voltage waveforms obtained from winding f_a for inputs that satisfy the bridge function are shown in Fig. 4(a). Typical noise outputs that are obtained when the inputs do not satisfy the



(a)

(b)

Fig. 4—Signal and noise outputs for the structure shown in Fig. 3(a). (Time scale = 0.5 μs/division. Voltage scale = .05 volt/division.)

bridge function appear in Fig. 4(b). The inequality of output amplitudes in Fig. 4(a) are thought to be caused by inhomogeneities in the magnetic material.

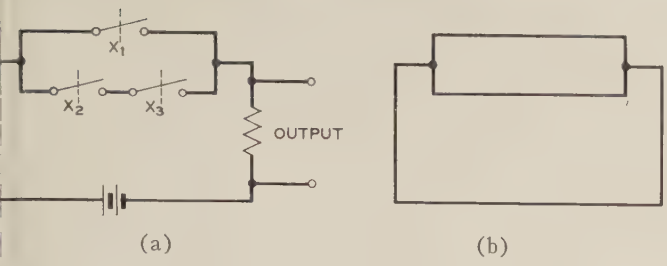
III. Second Method

In the second procedure the electrical paths of the relay structure are considered to be replaced by flux paths, having cross sections apportioned so that a reset pulse will saturate the entire structure. The manner of application of the windings, representing the variables, is determined by reference to the relay structure. As before, a current in a variable winding will inhibit flux switching through a particular part of the structure. The technique will be illustrated by use of the following simple example.

Consider the simple relay structure shown in Fig. 5(a), and consider the consequences of the following procedure: Use Fig. 5(a) to establish the general topology of the corresponding magnetic structure as indicated in Fig. 5(b). Next apportion the cross sections suitably, and place a drive and a reset winding on the common return path as shown in Fig. 6(a). It remains to apply the windings to carry the variables.

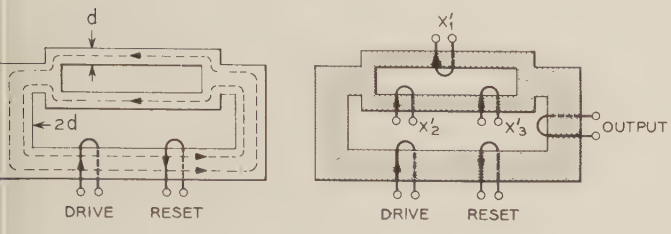
To appreciate the manner of application of the windings, consider the proposed method of operation. First the reset current will be applied so as to establish the flux pattern shown in Fig. 6(a). In a sense the structure is then "charged," all flux paths being saturated. The drive and variable currents will then be applied simultaneously, with the drive acting to completely reverse the flux pattern.

In the relay structure shown in Fig. 5(a), the top path will not carry current when X_1 is absent. Thus, in the magnetic analog [Fig. 6(a)] the top flux path should not carry switching flux if X_1 is absent. This suggests blocking the top flux path by applying X_1' as in Fig. 6(b). Hence, whenever a current is present in this wind-



(a) (b)

Fig. 5—Given relay structure and the first step in establishing its magnetic analog.



(a) (b)

Fig. 6—(a) Structure with apportioned area. (b) The final magnetic structure.

hg, flux switching through this path will be inhibited. The other windings may be applied, in a similar manner, as shown in Fig. 6(b). Suppose in this structure that $X_1=1$, $X_2=1$, $X_3=0$. Then, when the drive and variables are applied, X_3' will prevent switching in the middle path. However, the top path will carry switching flux, giving rise to a voltage in the output winding. A similar argument holds when the input variables take on different values. If this argument is carried through it is easy to see that the magnetic structure in Fig. 6(b) realizes the same logical operation as the relay structure in Fig. 5(a).

With the above example in mind, it is apparent that the general procedure for establishing a magnetic analog may be summarized as follows:

1) Establish the topology.
2) Apportion the areas, apply drive, and reset windings. The apportioning is not unique, but it is very easy to obtain at least one possible structure.
3) Put on a winding corresponding to each relay contact.
4) Simplify the structure so as to realize particular requirements, *e.g.*, to minimize the number of windings.

For experimental purposes the analog of the relay tree shown in Fig. 7 was tested. The straightforward analog is shown in Fig. 8. A simplified structure having the same topology is shown in Fig. 9.

Although the structure in Fig. 9 was arrived at by establishing a correspondence between relay circuits and magnetic circuits, the operating principles are similar to those of the laddic.

Consider the operation of the structure shown in Fig. (b) when X_1 and X_2 both take on the value 1. First the reset establishes the flux pattern shown in Fig. 8(a). The

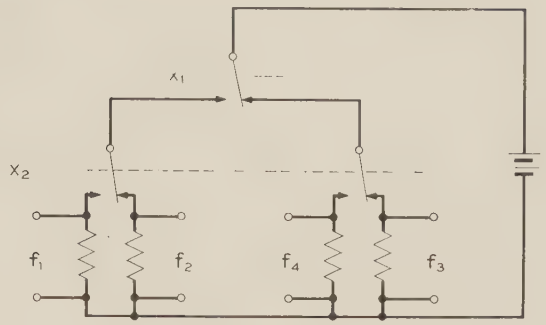
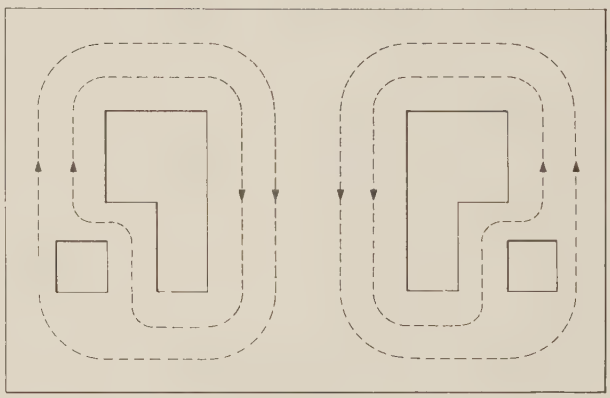
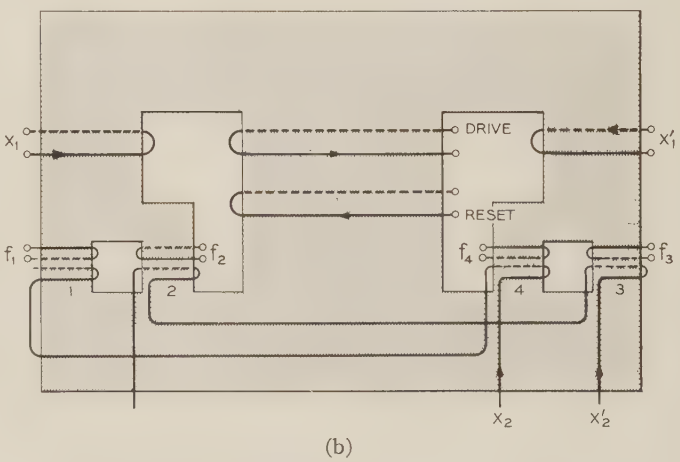


Fig. 7—Relay tree.



(a)



(b)

Fig. 8—Analog of the relay tree.

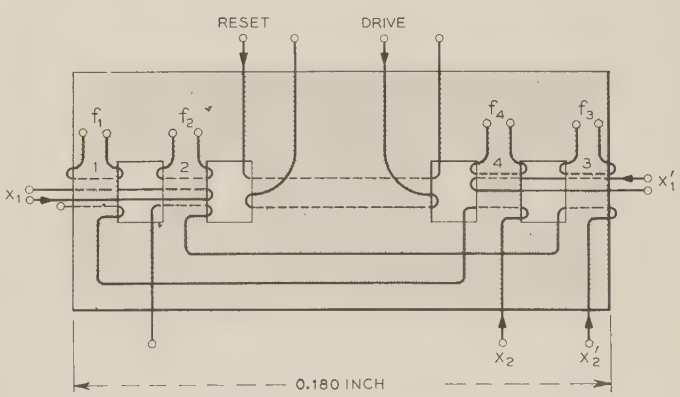


Fig. 9—Experimental structure.

drive and variables are then applied simultaneously. Provided the current in X_1 is sufficiently large, the left-hand half of the structure will be held in the saturated condition. Flux can then switch in the right half of the structure only. If X_2 is present, then rung 4 will be held in the saturated condition, and the only rung through which flux can be switched will be rung 3. Flux will be switched through output rung 3 if and only if the input variables have value $X_1=1$, $X_2=1$, and for this input no other output will be obtained. Similar unique outputs are obtained on rungs 1, 2, and 4 for inputs $X_1'X_2'$, $X_1'X_2$, X_1X_2', respectively.

Fig. 10(a) shows the output voltages across the four output rungs for the condition $X_1=1$, $X_2=1$. Fig. 10(b) shows the output voltages across the four output rungs for the condition $X_1=1$, $X_2=0$. Note that on a particular rung the noise and signal are of opposite polarity.[6] This will be seen to be reasonable if the mmf acting on the rung, under switching and nonswitching conditions, is examined. This result will be true in general for structures derived using this technique.

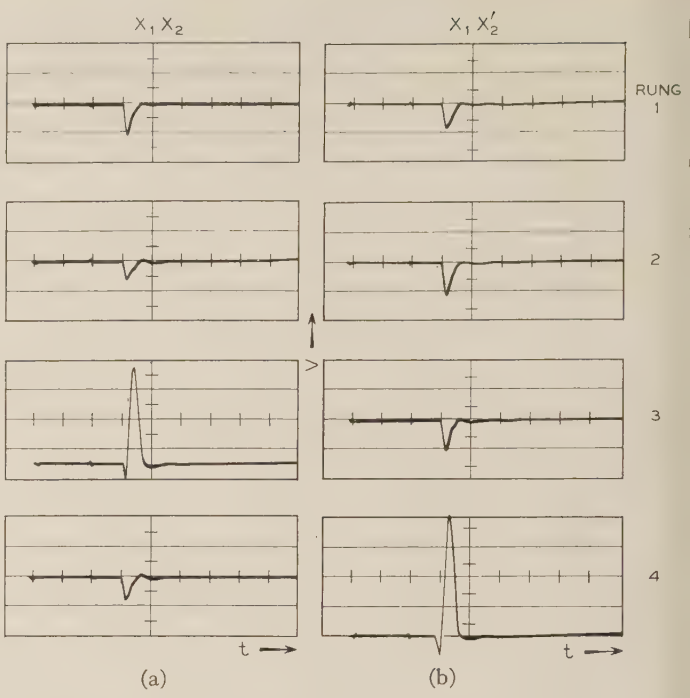


Fig. 10—Output waveforms obtained from the structure shown in Fig. 9. (Time scale = 1.0 μs/division. Voltage scale = 0.1 volts/division.)

IV. Discussion

It is apparent that the two methods described lead to different magnetic analogs for a given circuit, although there are similarities in the basic principle of operation. The first method may sometimes lead to a more compact structure because all paths may have the same small cross section. On the other hand, the reset winding required for the second method is much simpler. Perhaps of greater importance is the fact that the first method alone can be used to realize bridge-type circuits using a planar structure. However, neither analog appears to be generally superior to the other when only series-parallel circuits are considered.

Using either type of circuit, the currents representing the variables have a minimum value for a given drive current, but there is no significant maximum value. Thus, margins are large, as is the case for the laddic.

In the example discussed in Section II, the output was taken using the laddic principle, namely, a flux reversal was obtained through the output linkage only when the intermediate paths are all blocked. In the example of Section III, however, the output used is similar to the negation output of the laddic.[1] Clearly either output can be used in the two cases. Some modifications of the circuit are required but the idea is basically the same. The normal laddic-type output is to be preferred from some points of view since the output waveform for a "1" remains the same for all of the appropriate input combinations. The "0" output is typically small. The negation-type output may give different output waveforms for the different input combinations for a "1," because the switching paths, and hence switching speeds, may vary. On the other hand the output for a "0" will have the opposite polarity to that for a "1," and this may be advantageous for some applications.

As was previously pointed out, these more complicated structures may lead to logic circuits which are simpler in some respects than the equivalent laddic circuit. One example was given in Section II, where it was shown that the more complicated magnetic structure gave an appreciable reduction in variable windings. It may well be that simplifications of this nature could give a significant reduction in cost.

No attention has been given in this paper to the current drives necessary or to the switching speeds involved. These may be derived for any particular geometry by applying the design formulas described previously.[1]

V. Standard Structures

It is of interest to note that the analog of the relay tree discussed in Section III, or, similarly, its analog derived according to the method of Section II, may also be used as a standard structure. The reason is that outputs taken from the final branches of the tree, for example the four outputs shown in Fig. 9, separately give a different conjunctive form of the input variables, and jointly give all of the possible conjunctive forms. Any Boolean expression can be expressed in the so-called disjunctive canonical form, namely

$$(x_{11}x_{12}\cdots x_{1n}) + (x_{21}x_{22}\cdots x_{2n}) + \cdots,$$

[6] It should be noted that the waveforms in Fig. 10 do not show the noise pulse that is produced at the end of the applied current pulse. This pulse will have the same polarity as the signal, but may be made negligible in amplitude by increasing the decay time of the applied pulse. Referring to Fig. 10, the small negative signal that precedes the "1" waveform is believed to be attributable to stray coupling in the circuit.

where the x's may represent the variables or the negations. Thus, it follows that in principle any Boolean function can be realized by an output winding which links the appropriate number of the branches of the tree.

In essence the tree structure is complementary to the paddic, which gives an output of the conjunctive canonical form.

ACKNOWLEDGMENT

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The Determination of Carry Propagation Length for Binary Addition*

GEORGE W. REITWIESNER†

Summary—It is well known that the expected maximum length of nonzero carry propagation in the addition of two uniformly distributed binary numbers of n-digits each is less than $\log_2 n$. The propagation of both zero and nonzero carry is required in the employment of asynchronous self-timing addition. For the addition of two n-digit binary numbers which are uniformly distributed, a simple recursive algorithm is readily derived for the exact determination of the expected maximum length of zero or nonzero carry propagation.

IN 1946 Burks, Goldstine, and von Neumann published[1] a proof that the expected maximum length of carry propagation in the addition of two binary numbers of n digits each does not exceed $\log_2 n$. In 1955 Gilchrist, Pomerene, and Wong exhibited[2] a logical design whereby a signal for the completion of addition is derived from the fact of the completion of all carry propagation, including, of course, the longest. The former paper considered the propagation of only nonzero carry; of necessity, the latter paper considered the propagation of both zero and nonzero carry.

In the following argument a formula is derived for the determination of the expected maximum length of zero or nonzero carry propagation in the addition of two binary numbers of n digits each.

Argument is conducted for numbers X which are expressed in 2's-complement representation in the range $-1 \leq X < 1$ by n binary digits $x_i = 0, 1$ $(i = 0, 1, \cdots n-1)$ as

$$X = -x_0 + \sum_{1}^{n-1} x_i 2^{-i}. \tag{1}$$

Since 2's-complement arithmetical operation is distinguished by the replacement, during the detailed implementation of addition, of numbers X by their residues X^*, modulo 2, which lie in the range $0 \leq X^* < 2$ and which are expressed as

$$X^* = \sum_{0}^{n-1} x_i 2^{-i}, \tag{2}$$

argument is restricted to the formation of the sum, modulo 2, of two residues X^* modulo 2. Employing, in place of the generic X and x_i, the notation A and a_i to denote the augend, B and b_i to denote the addend and S and s_i to denote the sum, argument is thus restricted to the formation of

$$S^* = A^* + B^*, \qquad \text{modulo 2}, \tag{3}$$

according to a recursion of the general form

$$c_{n-1} = 0 \tag{4n}$$

$$\left.\begin{aligned} h_i &= a_i \oplus b_i \\ c_{i-1} &= a_i b_i \vee h_i c_i \\ s_i &= h_i \oplus c_i \end{aligned}\right\} \quad i = n-1, n-2, \cdots, 0 \tag{4h, 4c, 4s}$$

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[1] A. W. Burks, H. H. Goldstine and J. von Neumann, "Preliminary Discussion of the Logical Design of an Electronic Computing Instrument," Inst. for Advanced Study, Princeton, N. J.; June, 1946.

[2] B. Gilchrist, J. H. Pomerene and S. Y. Wong, "Fast carry logic for digital computers," IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-4, pp. 133–136; December, 1955.

where all quantities a_i, b_i, h_i, c_i, s_i are binary digits, where $\vee$ denotes the INCLUSIVE OR, where $\oplus$ denotes the EXCLUSIVE OR, where c_i represents carry, and where c_{-1} is superflous because of the modulo 2 feature and 2's-complement addition. Since argument here is concerned only with carry propagation, (4s) is hereinafter essentially ignored.

Through the familiar device of complementing c_{n-1} and the b_i, argument extends, implicitly, to accommodate subtraction as well as addition.

Those portions of the following discussion which employ statistical argument are founded upon the hypothesis that each a_i and b_i assumes each of the values 0 and 1 with independent probability $\frac{1}{2}$. That this hypothesis thoroughly represents reality is not contended; however, it is adopted here as a first approximation to reality.

In the sense of the paper of Gilchrist, Pomerene, and Wong: the binary digits u_i and v_i ($i=-1, 0, \cdots, n-1$) are defined as

$$\left.\begin{aligned} u_i &= 1 \text{ if } c_i = 0 \text{ has been ascertained} \\ u_i &= 0 \text{ if } c_i = 0 \text{ has not yet been ascertained} \\ v_i &= 1 \text{ if } c_i = 1 \text{ has been ascertained} \\ v_i &= 0 \text{ if } c_i = 1 \text{ has not yet been ascertained} \end{aligned}\right\} \quad (5)$$

(clearly u_i and v_i apply for zero and nonzero carry, respectively); and (4n, h, c) is re-expressed as

$$1 = u_{n-1} \neq v_{n-1} = 0 \quad (6n)$$

$$1 = u_{i-1} \neq v_{i-1} = 0 \quad \text{for} \quad a_i = b_i = 0 \quad (6i0)$$

$$0 = u_{i-1} = v_{i-1} = 0 \quad \text{for} \quad a_i \neq b_i \quad (6i\neq)$$

$$0 = u_{i-1} \neq v_{i-1} = 1 \quad \text{for} \quad a_i = b_i = 1 \quad (6i1)$$

$$h_i = a_i \oplus b_i \quad (6h)$$

$$u_{i-1} = h_i u_i \quad \text{for} \quad h_i = 1 \quad (6cu)$$

$$v_{i-1} = h_i v_i \quad \text{for} \quad h_i = 1 \quad (6cv)$$

for $i=n-1, n-2, \cdots, 0$, where (6n), (6i), and (6h) represent initial conditions and (6c) represents a set of recursions which may change the values of particular u_i and v_i from those established under (6i). Trivially, $u_i=1=v_i$ is impossible for any i, and ultimately $u_i \neq v_i$ must apply for every i. Thus, for the definition of the binary digit $w_i (i=-1, 0, \cdots, n-1)$ as

$$w_i = u_i \vee v_i, \quad (7)$$

the completion of all (zero and nonzero) carry propagation is signalled by the condition

$$\text{all} \quad w_i = 1, \quad (8)$$

the recognition of which may serve as a signal for the completion of addition through the employment of either v_i or $1-u_i$ for c_i in (4s). (As for c_{-1}, the digits u_{-1}, v_{-1}, and w_{-1} are superflous in the modulo 2 addition of A^* and B^*.)

It is readily apparent: that any recursion (6c) must terminate upon recognition of $h_i=0$, which embraces both conditions (6i0) and (6i1) for the initiation of a recursion (6c); that at most one of the expressions (6cu) and (6cv) applies for any particular value of i; and that all applicable recursions (6c) may be executed concurrently—whence the duration of carry propagation is governed by the longest carry propagation recursion (6c) for any particular addition.

Assigning one unit for the establishment of the initial conditions (6n, i, h) and one unit for each iteration of any recursion (6c), a (zero or nonzero) carry-sequence of length exactly L is defined to exist when exactly $L-1$ iterations of a recursion (6c) are necessary to exhaust a sequence of consecutively indexed $h_i=1$.

Ensuing argument will operate by induction over an index $m=1, 2, \cdots, n$.

In the addition of the two m-digit numbers

$$\sum_{n-m}^{n-1} a_i \cdot 2^{-i} \quad \text{and} \quad \sum_{n-m}^{n-1} b_i \cdot 2^{-i} \quad (9)$$

according to (6) and (4s) for $i=n-1, n-2, \cdots, n-m$, the total number of possible cases (combinations of values of a_i and b_i) is clearly 2^{2m}; and among all 2^{2m} cases, the maximum carry-sequence length is at least 1 (for all $h_i=0$) and at most $m+1$ (for all $h_i=1$). Employing the index j to denote the maximum carry-sequence length in the addition of the two m-digit numbers (9), the 2^{2m} cases are separated into $m+1$ categories according to the values assumed by $j=1, 2, \cdots, m+1$, and the number of cases in each category is accordingly denoted $P_{m,j}$. Thus, trivially,

$$\sum_{1}^{m+1} P_{m,j} = 2^{2m}; \quad (10)$$

and under the assumed stochastic hypothesis it readily follows that the expected length E_m of the longest carry sequence in the addition of the two m-digit numbers (9) is given by

$$E_m = \sum_{1}^{m+1} j \cdot P_{m,j} \cdot 2^{-2m}. \quad (11)$$

The objective of argument is the evaluation of (11) for $m=n$.

In the addition of the two m-digit numbers (9), the leading carry sequence is defined as that carry sequence which includes (ultimately) $u_{n-m-1}=1$ or $v_{n-m-1}=1$; and among all 2^{2m} cases, the leading carry-sequence length is at least 1 (for $h_{n-m}=0$) and at most $m+1$ (for all $h_i=1$). Employing the index k to denote the leading carry-sequence length, the $P_{m,j}$ cases in each category defined above are separated into j subcategories according to the values assumed by $k=1, 2, \cdots, j$, and the number of cases in each subcategory is accordingly denoted $Q_{m,j,k}$.

Thus, trivially,

$$P_{m,j} = \sum_{1}^{j} Q_{m,j,k}. \tag{12}$$

The object of argument will be achieved through: 1) expressing the $Q_{m,j,k}$ in terms of the $P_{m-1,j}$ and $Q_{m-1,j,k}$ for $m=2, 3, \cdots, n$; 2) employing (12) to evaluate the $P_{m,j}$ for $m=2,3, \cdots, n$; and 3) employing (11) for $m=n$ to evaluate E_n.

Of necessity, (as illustrated in Table I)

$$\left.\begin{aligned} Q_{m,j,k} &= 0 \quad \text{for} \quad j < k \\ Q_{m,j,k} &= 0 \quad \text{for} \quad m+1-j < k < j. \end{aligned}\right\} \tag{13}$$

The required expression for the $Q_{m,j,k}$ in terms of the $P_{m-1,j}$ and $Q_{m-1,j,k}$ is the recursion

$$Q_{m,j,1} = 2P_{m-1,j} \qquad 1 \le j \le m+1 \tag{14-1}$$

$$Q_{m,j,k} = 2Q_{m-1,j,k-1} \qquad 2 \le k < j \le m+1 \tag{14-k}$$

$$Q_{m,j,j} = 2(Q_{m-1,j-1,j-1} + Q_{m-1,j,j-1}) \qquad 2 \le j \le m+1 \tag{14-j}$$

For the initial conditions (for $m=1$)

$$Q_{1,1,1} = 2 \tag{15-1}$$

$$Q_{1,2,2} = 2. \tag{15-2}$$

The initial conditions (15) are readily established by separating the $2^2=4$ cases for $m=1$ into two categories according to $j=1$ and $j=2$: the condition $j=1$ occurs only for $a_{n-1}=b_{n-1}$, which occurs two ways, whence follows (15-1); and the condition $j=2$ occurs only for $a_{n-1}\neq b_{n-1}$, which occurs two ways, whence follows (15-2). The validity of recursion (14) is observed when argument is separated according to $a_{n-m}=b_{n-m}$ for (14-1) and $a_{n-m}\neq b_{n-m}$ for (14-k) and (14-j); it is patently clear that the leading carry sequence has length $k=1$ when $a_{n-m}=b_{n-m}$, which occurs two ways, and has length $k>1$ when $a_{n-m}\neq b_{n-m}$, which occurs two ways. The transition from $m-1$ to m in (14) corresponds to increasing by 1 the number of digits employed in defining the two numbers (9). For $a_{n-m}=b_{n-m}$, there applies only $k=1$, whence, for each length $j=1, 2, \cdots, m$ of the longest carry sequence among the $m-1$ highest-indexed a_i and b_i, there follows (14-1), wherein $P_{m-1,m+1}=0$ is tacitly understood.

For $a_{n-m}\neq b_{n-m}$, argument is further separated according to $k<j$ or $k=j$. If the length of the leading carry sequence is at least 2 less than the length of the longest carry sequence among the $m-1$ highest-indexed a_i and b_i, then, in the transition from $m-1$ to m for $a_{n-m}\neq b_{n-m}$, the length of the leading carry sequence will increase by 1 but cannot become equal to the length of the longest carry sequence, whence there applies (14-k), wherein $Q_{m-1,m+1,k-1}=0$ is tacitly understood. And if the length of the leading carry sequence is equal to or less by 1 than the length of the longest carry sequence among the $m-1$ highest-indexed a_i and b_i, then, in the transition from $m-1$ to m for $a_{n-m}\neq b_{n-m}$, the length of the leading carry sequence will increase by 1 and will be equal to the length of the longest carry sequence, whence there applies (14-j).

The objective of argument is achieved through (15), through (14) and (12) for $m=2, 3, \cdots, n$, and through (11) for $m=n$. An upper bound of 2^{2m} readily applies for the $Q_{m,j,k}$ and $P_{m,j}$ as a consequence of (10); however, the entire argument readily is rephrased to employ numbers which do not exceed 2^m by discarding the factor 2^m which exists in each $Q_{m,j,k}$ and $P_{m,j}$ because of (15) and the factors 2 in (14).

For the definitions

$$\begin{aligned} \overline{Q}_{m,j,k} &= 2^{-m}Q_{m,j,k} \\ \overline{P}_{m,j} &= 2^{-m}P_{m,j}, \end{aligned} \tag{16}$$

(11), (12), (14), and (15) yield, respectively,

$$E_m = \sum_{1}^{m+1} j \cdot \overline{P}_{m,j} \cdot 2^{-m} \tag{17}$$

and

$$\overline{P}_{m,j} \sum_{1}^{j} \overline{Q}_{m,j,k} \tag{18}$$

and the recursion

$$\overline{Q}_{m,j,1} = \overline{P}_{m-1,j} \qquad 1 \le j \le m+1 \tag{19-1}$$

$$\overline{Q}_{m,j,k} = \overline{Q}_{m-1,j,k-1} \qquad 2 \le k < j \le m+1 \tag{19-k}$$

$$\overline{Q}_{m,j,j} = \overline{Q}_{m-1,j-1,j-1} + \overline{Q}_{m-1,j,j-1} \qquad 2 \le j \le m+1 \tag{19-j}$$

for the initial conditions

$$\begin{aligned} \overline{Q}_{1,1,1} &= 1 \\ \overline{Q}_{1,2,2} &= 1, \end{aligned} \tag{20}$$

where, of necessity, (13) applies for $\overline{Q}_{m,j,k}$ in place of $Q_{m,j,k}$.

Thus, E_n is evaluated through (20), through (19) and (18) for $m=2, 3, \cdots n$, and through (17) for $m=n$, employing numbers $\overline{Q}_{m,j,k}$ and $\overline{P}_{m,j}$ which lie in the range $0\le\overline{Q}_{m,j,k}, \overline{P}_{m,j}\le 2^m$.

The values of the $\overline{Q}_{m,j,k}$ and $\overline{P}_{m,j}$ for $1\le m\le 7$ and of the E_n for $2\le n\le 39$ are listed in Tables I and II; and the values of the E_n and of $\log_2 n$ for $2\le n\le 39$ are shown in Fig. 1. As an item of passing interest, it is observed that the two curves in the figure are roughly parallel. That E_n (which is determined for both zero and nonzero carry propagation) exceeds $\log_2 n$ is not inconsistent with the result obtained by Burks, Goldstein, and von Neumann (which was derived for only nonzero carry propagation).

Clearly, (19) and (18) and (17) are of very simple form, and (13) for $\overline{Q}_{m,j,k}$ in place of $Q_{m,j,k}$ reveals that the execution of (19) and (18) by calculating machine is tractable employing essentially $(n/2)^2$ storage locations for numerical data. The E_n for $2\le n\le 39$ were computed in a few moments by the EDVAC.

TABLE I

m	j	$\bar{P}_{m,j}$	$\bar{Q}_{m,j,k}$							
			$k=1$	2	3	4	5	6	7	8
1	1	1	1							
	2	1		1						
2	1	1	1							
	2	2	1	1						
	3	1			1					
3	1	1	1							
	2	4	2	2						
	3	2	1		1					
	4	1				1				
4	1	1	1							
	2	7	4	3						
	3	5	2	1						
	4	2	1		1	1				
	5	1					1			
5	1	1	1							
	2	12	7	5						
	3	11	5	2	4					
	4	5	2	1		2				
	5	2	1				1			
	6	1						1		
6	1	1	1							
	2	20	12	8						
	3	23	11	5	7					
	4	12	5	2	1	4				
	5	5	2	1			2			
	6	2	1					1		
	7	1							1	
7	1	1	1							
	2	33	20	13						
	3	47	23	11	13					
	4	27	12	5	2	8				
	5	12	5	2	1		4			
	6	5	2	1				2		
	7	2	1						1	
	8	1								1

TABLE II

n	E_n
2	2.000
3	2.375
4	2.688
5	2.938
6	3.156
7	3.344
8	3.512
9	3.662
10	3.799
11	3.924
12	4.039
13	4.146
14	4.245
15	4.338
16	4.425
17	4.508
18	4.585
19	4.659
20	4.729
21	4.796
22	4.860
23	4.921
24	4.980
25	5.036
26	5.091
27	5.143
28	5.193
29	5.242
30	5.289
31	5.335
32	5.380
33	5.423
34	5.464
35	5.505
36	5.544
37	5.583
38	5.620
39	5.657

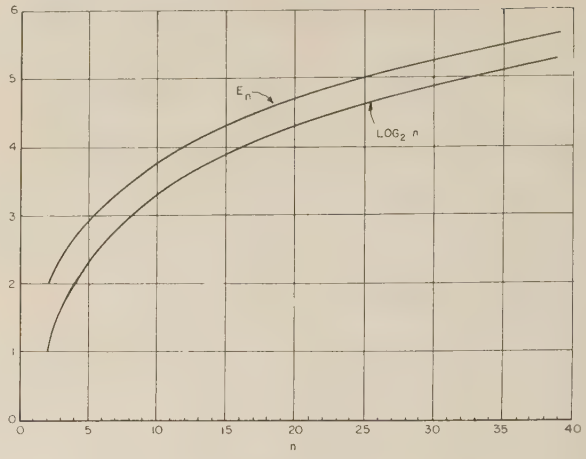

Fig. 1.

Regular Expressions and State Graphs for Automata*

R. McNAUGHTON† AND H. YAMADA†

Summary—Algorithms are presented for 1) converting a state graph describing the behavior of an automaton to a regular expression describing the behavior of the same automaton (section 2), and 2) for converting a regular expression into a state graph (sections 3 and 4). These algorithms are justified by theorems, and examples are given. The first section contains a brief introduction to state graphs and the regular-expression language.

I. Terminology, Notation, and Fundamental Theorems

IN this paper a state graph for a one-input, one-output automaton consists of a number of circles connected with arrows, each arrow being labeled 0 or 1, or both. Each circle shall have exactly one arrow leaving it labeled 0, and exactly one labeled 1, leading either back to the same circle or to another circle. Some circles (double circles) have within them a slightly smaller concentric circle while others (single circles) do not. The graph has a single unlabeled arrow pointing to one of the circles, but not leading *from* any circle. The single circles represent states, transitions into which yield an output 0; the double circles represent states, transitions into which yield an output of 1. The unlabeled arrow points to the initial state. These state graphs, like those of Moore,[1] have a single output associated with each state. Unlike the treatment in his work, however, the output of an automata in this paper occurs during the transition into a state, not when the automaton is in the state. Thus, the output of the initial state is not necessarily the first output of the output sequence. For example, if the input sequence 101001111 is applied to automaton described by the graph of Fig. 1, then the output sequence is 001110101. This type of state graph makes for convenience in the algorithms of the later sections.

Regular expressions are introduced which denote classes of sequences of zeros and ones, and which describe the behavior of automata. A sequence of zeros and ones is thought of as an input sequence of an automaton. The manner in which a regular expression describes the behavior of an automaton is described below. Before that, a precise definition of "regular expression" is given, followed by a precise account of how a regular expression denotes a class of sequences of zeros and ones.

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[1] E. F. Moore, "Gedanken experiments on sequential machines," "Automata Studies," C. E. Shannon and J. McCarthy, Eds., Princeton, N. J., pp. 1–29–156; 1956.

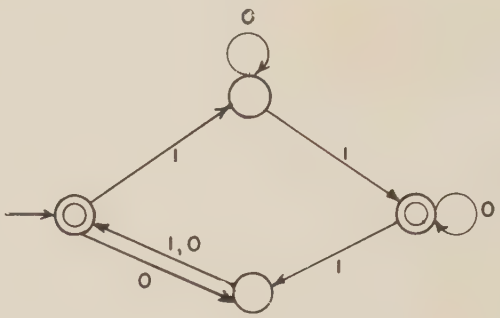

Fig. 1.

Regular Expressions

The regular-expression language (adapted from Kleene[2] and Copi, Elgot, and Wright,[3] has the symbols zero (0), one (1), star (*), dot (·), cup (∪), cap (∩), tilde (∼), (upper-case) lambda (Λ), (lower-case) phi (ϕ), and parentheses. Zero and one are digits. Digits, lambda, and phi are term signs. Star, dot, cup, cap, and tilde are the operator signs. Parentheses are used for grouping.

"Regular expression" is defined recursively as follows:

1) A string consisting of a single zero, a single one, a single lambda, or a single phi is a regular expression.

2) If $\beta_1, \cdots, \beta_n$ are regular expressions then so are $(\beta_1)^*$, $(\beta_1)\cdot(\beta_2)\cdot\cdots\cdot(\beta_n)$, $(\beta_1)\cup(\beta_2)\cup\cdots\cup(\beta_n)$, $(\beta_1)\cap\cdots\cap(\beta_n)$, and $\sim(\beta_1)$.

3) No string is a regular expression unless its being so follows from 1) and 2).

In practice the dot will be omitted completely. For convenience, parentheses will sometimes be omitted, in a systematic fashion, by specifying the order of strength of the various operator signs. Cup and cap have the greatest strength and are equal in strength; next is the dot; finally the tilde and star have the least strength. Thus $0\cup10$ is short for $0\cup1\cdot0$. In the latter the cup has greater strength than the dot, so that the terms joined by the dot are grouped together before terms are grouped by the cup. Thus the fully unabbreviated form is $(0)\cup[(1)\cdot(0)]$. Similarly, $0\cup\sim0$, $0\cap0^*$, 00^* and ~00 are to be interpreted, respectively as $(0)\cup[\sim(0)]$, $(0)\cap[(0)^*]$, $(0)\cdot[(0^*)]$ and $[\sim(0)]\cdot(0)$. No parentheses in $(0\cup1)(00)^*$ may be omitted.

[2] S. C. Kleene, "Realization of events in nerve nets and finite automata," in "Automata Studies," C. E. Shannon and J. McCarthy, Eds., Princeton, N. J., pp. 3–42; 1956.

[3] I. M. Copi, C. L. Elgot, and J. B. Wright, "Realization of events by logical nets," *J. Assoc. Comp. Mach.*, vol. 5, pp. 181–196; April, 1958.

Sequences

Regular expressions are used to denote sequences of zeros and ones. The *length* of a sequence is the number of terms (zeros and ones) in it. If $\sigma_1, \cdots, \sigma_n$ are finite sequences of zeros and ones whose lengths are $l_1, \cdots, l_n$, respectively, then the *concatenation* of $\sigma_1, \cdots, \sigma_n$ is the sequence σ of length $l_1+\cdots+l_n$, such that, for each i, $1 \leqq i \leqq n$, the $(l_1+\cdots+l_{i-1}+1)$th through the $(l_1+\cdots+l_i)$th terms are those of σ_i in order. Note that the concatenation of σ_1, σ_2 is different from the concatenation of σ_2, σ_1. If σ_1, or σ_2, is the null sequence (whose length is zero), then the concatenation of σ_1, σ_2 is σ_2, or σ_1, respectively.

A regular expression denotes both sequences and classes of sequences. Since a regular expression denotes only a single class of sequences and denotes a sequence if, and only if, the sequence is a member of that class, no confusion will result. The recursive characterization of denotation is as follows:

1) If a regular expression denotes a class of sequences, then it denotes any sequence in that class.

2) The regular expression 0 and the regular expression 1 denote, respectively, the unit class of the sequence of a single zero and the unit class of the sequence of a single one. (A unit class of an entity is the class whose only member is that entity.)

3) The regular expression ϕ denotes the unit class of the null sequence, *i.e.*, the sequence of zero length.

4) The regular expression Λ denotes the null class of sequences.

5) The regular expression β^* denotes the smallest class of sequences which contains the null sequence and contains, for any σ_1 denoted by β^* and σ_2 denoted by β, the concatenation of σ_1, σ_2. In other words, β^* denotes the class of all sequences σ such that, for some non-negative integer n (zero included!), σ is the concatenation of n sequences (not necessarily distinct and not necessarily identical), each of which is denoted by β.

6) The regular expression $\beta_1 \cup \beta_2 \cup \cdots \cup \beta_n$ denotes the union of the classes denoted by $\beta_1, \beta_2, \cdots, \beta_n$.

7) The regular expression $\beta_1 \cap \beta_2 \cap \cdots \cap \beta_n$ denotes their intersection.

8) The regular expression $\beta_1\beta_2\cdots\beta_n$ denotes the class of all σ's such that there exist sequences $\sigma_1, \cdots, \sigma_n$, where, for each i, σ_i is denoted by β_i, and σ is the concatenation of $\sigma_1, \cdots, \sigma_n$.

9) The regular expression $\sim\beta$ denotes the complement of the class denoted by β with respect to the class of all finite sequences of zero and ones.

10) A regular expression does not denote anything unless its doing so follows from 1) through 9).

Thus, for example, $00 \cup 11$ denotes the class whose members are just the two sequences 00 and 11. And $(00 \cup 11)^*$ denotes the infinite class whose members are the empty sequence, 00, 11, 0000, 0011, 1100, 1111, 000000, 000011, etc.

Note that lambda is used here to denote the empty class of sequences and not the empty sequence as it sometimes does in the literature in information theory. That the empty sequence and the empty class of sequences must be distinguished is apparent because of the different ways they occur in the equations at the end of this section.

Two regular expressions α and β are equal $(\alpha=\beta)$ if they denote the same class.

Automata

A regular expression α describes (the behavior of) a one-input, one-output automaton when, for every $t \geqq 1$, the output at time t is 1, if and only if the input sequence from time 1 through time t inclusive is denoted by α. Note that, according to this point of view, an automaton cannot respond to the null sequence of inputs. This results from our characterization of state graphs, in which the initial state does not necessarily yield an output. As a consequence, we have an important principle: a regular expression α describes the behavior of an automaton if and only if $\phi \cup \alpha$ describes its behavior.

Although only automata with one binary input and one binary output are considered, the results of this paper can be applied to automata with more than two input states and more than two output states. As far as state graphs are concerned, this fact is apparent from the literature. A regular expression can describe the behavior of an automaton with n input states if it uses the symbols $2, 3, \cdots, n-1$ as well as 0 and 1 as digits. If the automaton has more than two output states, however, the matter is not that easy. In this case, the only method seems to be to assume that there are b binary outputs, and to have a separate regular expression describing each. The regular-expression language seems most suitable for automata with only one binary output.

As an example, consider the modulo-two one's counter, whose state graph is shown in Fig. 2; its output is 1 at time t if, and only if, the input is 1 at time t and there have been an even number of 1's up to and including time t in the input sequence. A regular expression describing this automaton is $(0^*10^*1)^*$.

It will follow from the results of sections II, III, and IV that every regular expression describes a finite automaton and that every finite automaton is described by some regular expression. It also follows that regular expressions that contain no tilde, cap, lambda, or phi, are sufficient to describe all automata, except the trivial automaton described by Λ, which produces a zero output at all times regardless of the input sequence. This result and its converse appeared in Kleene's article,[2] and is further clarified by Copi, Elgot, and Wright.[3] The extension of this result to all regular expressions is a fairly easy matter, and requires far less effort than the con-

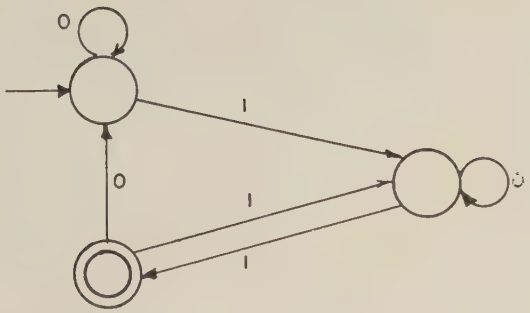

Fig. 2.

ents of sections II, III, and IV. (The verification of this act we leave to the reader.) The purpose of those sections is the presentation of efficient ways of converting rom regular-expression description of automata to tate-graph description, and vice versa.

Specification Language for Automata

The process of logic design is one that starts with a pecification of what a logic circuit must do in the way of haracterizing how the circuit responds with outputs to nputs. This specification must be precise, in order to roduce by the process of logic design a result that is anted.

We are of the opinion that the regular-expression anguage as presented here is a good language for such pecifications. It has three virtues. First, in contrast to he state-graph language, its descriptions can be conveniently written out in a line from left to right. Second, t is precise and formal, as opposed, for example, to natural languages such as English. Third, there is indication that one who is trained in using the language can eadily, that is, without computation or excessive reflection, express ideas in this language. This last virtue is an important one. The regular expression language without he tilde, cap, phi, and lambda (which was the language developed by Kleene[2] and Copi, Elgot, and Wright[3]) does not have this virtue, or has it to a lesser legree.

As an example, consider the problem of designing an automaton that has an output 1 at time t if and only if either there have never been three consecutive zeros in he input sequence up to and including time t, or there have been three consecutive ones in the input sequence since the last three consecutive zeros. A regular expression specifying the automaton can readily be determined. Noting that $(0\cup1)^*$ denotes the class of all finite sequences (of zeros and ones), and that $(0\cup1)^*000(0\cup1)^*$ denotes the class of all finite sequences having hree consecutive zeros somewhere, the desired regular expression is

$$\sim[(0\cup1)^*000(0\cup1)^*]\cup(0\cup1)^*111\sim[(0\cup1)^*000(0\cup1)^*].$$

One can express this idea without the tilde, noting after some reflection that $(1\cup01\cup001)^*(\phi\cup0\cup00)$ denotes the class of all finite sequences that do not have three consecutive zeros anywhere. But this is not what one thinks when one says, "a sequence without three consecutive zeros anywhere." In a certain sense $\sim[0\cup1)^*000(0\cup1)^*]$ is what one thinks when one utters that English phrase.

If we are justified in believing that this regular-expression language is a good specification language for automata, then the algorithm of sections III and IV of this paper are important. They provide a way of obtaining a state graph from any regular expression; from the state graph the automaton can be designed, depending on the physical means at the designers' disposal. In Copi, *et al.*,[3] a method is given (which is a modification of one appearing in Kleene[2]) for constructing a net consisting of "and" gates, "or" gates, inverters, and delay elements from a regular espression not containing tilde, cap, lambda, and phi. (A minor adjustment must be made since, in their terminology, α^* denotes the result of concatenating members of α *one* or more times, instead of *zero* or more times as used here.) There seems to be no way of extending that algorithm to regular expressions containing tilde and cap.

Some Regular-Expression Equations

The following can be verified by using the characterization of "denotation" and other principles presented in this section:

$$\alpha\beta\cup\alpha\gamma=\alpha(\beta\cup\gamma),$$

$$\beta\alpha\cup\gamma\alpha=(\beta\cup\gamma)\alpha,$$

$$(\alpha\cup\beta)^*=(\alpha^*\cup\beta^*)^*=(\alpha^*\beta^*)^*,$$

$$\phi\alpha=\alpha\phi=\alpha,$$

$$\phi^*=\phi,$$

$$\phi\cup\alpha^*=\alpha^*.$$

Any rule of Boolean Algebra holds for cup, cap, tilde, and lambda as union, intersection, complementation, and null set, respectively.

$$\Lambda^*=\phi,$$

$$\alpha\Lambda=\Lambda\alpha=\Lambda,$$

$$\sim((0\cup1)^*)=\Lambda,$$

$$\sim((0\cup1)(0\cup1)^*)=\phi,$$

$$\beta_1\cdots\beta_i\beta_{i+1}\cdots\beta_n=(\beta_1\cdots\beta_i)\beta_{i+1}\cdots\beta_n=\beta_1\cdots\beta_i(\beta_{i+1}\cdots\beta_n),\quad 1\leqq i\leqq n-1.$$

Note that the following pairs of regular expressions are not equal, as the accompanying counterexamples show.

$$\alpha\beta \cap \alpha\gamma, \qquad \alpha(\beta \cap \gamma). \tag{1}$$

Example:

$$\alpha = 0 \cup 00,$$
$$\beta = 0,$$
$$\gamma = 00.$$

$$(\alpha \cup \beta)^*, \qquad \alpha^* \cup \beta^*. \tag{2}$$

Example:

$$\alpha = 0,$$
$$\beta = 1.$$

$$(\alpha \cap \beta)^*, \qquad \alpha^* \cap \beta^*. \tag{3}$$

Example:

$$\alpha = 00,$$
$$\beta = 000.$$

II. An Algorithm for Constructing a Regular Expression from a State Graph

Let G be a state graph with n states $S_1, \cdots, S_n$. (S_1 is not necessarily the initial state.) Let $\alpha_{ij}{}^k$ be defined for all i, j, k such that $n \geqq k \geqq 0$, and $n \geqq i \geqq 1$, and $n \geqq j \geqq 1$, by induction on k as follows:

$\alpha_{i,j}{}^0 = 0 \cup 1$, if input 1 and input 0 both take G from S_i to S_j,
$= 0$, if input 0 but not input 1 takes G from S_i to S_j,
$= 1$, if input 1 but not input 0 takes G from S_i to S_j, and
$= \Lambda$, if neither 0 nor 1 takes G from S_i to S_j.

For $n \geqq k \geqq 1$, assume that $\alpha_{xy}{}^{k-1}$ has been defined for all x and y. Then

$$\alpha_{ij}{}^k = \alpha_{ij}{}^{k-1} \cup \alpha_{ik}{}^{k-1}(\alpha_{kk}{}^{k-1})^*\alpha_{kj}{}^{k-1}.$$

Theorem 2.1. $\alpha_{ij}{}^k$ denotes the class of all input sequences that take the state graph from S_i to S_j without going through S_x for any $x > k$. (Note the meaning of the word "through" here. If $i = 4$, $j = 10$, and the state graph goes from S_4 to S_{10} by means of the transition $S_4S_5S_4S_6S_8S_{10}$, then it goes through S_4 but not through S_{10}.)

The proof is by induction on k, following the recursive definition of $\alpha_{ij}{}^k$. For $k = 0$ it must be proved that $\alpha_{ij}{}^0$ denotes the class of sequences taking the graph from S_i to S_j without passing through any states at all. There are only two possible such sequences: the one-term sequence 0 and the one-term sequence 1. Hence, $\alpha_{ij}{}^0$ as defined, satisfies the condition of the theorem.

Assume now that $\alpha_{ij}{}^{k-1}$ satisfies the condition for all i and j. Each sequence taking the automaton of the state graph from S_i to S_j without causing it to pass through any S_x for $x > k$ could cause it to pass through S_k any number of times.

Case I. It causes it to pass through S_k zero times. Then the sequence is denoted by $\alpha_{ij}{}^{k-1}$, by inductive hypothesis; hence it is denoted by $\alpha_{ij}{}^k$ as constructed.

Case II. It causes it to pass through S_k exactly once. Let QR be the sequence, with Q the portion that leads from S_i to S_k, and R the portion that leads from S_k to S_j. Then Q is denoted by $\alpha_{ik}{}^{k-1}$, and R by $\alpha_{kj}{}^{k-1}$, by inductive hypothesis. Hence, by the meaning of the star, operator QR is denoted by $\alpha_{ik}{}^{k-1}(\alpha_{kk}{}^{k-1})^*\alpha_{kj}{}^{k-1}$ and, hence, by $\alpha_{ij}{}^k$ as constructed.

Case III. It causes it to pass through S_k more than once. Let QPR be the sequence, where Q is the portion taking it from S_i to S_k the first time, R is the portion taking it from S_k the last time to S_j, and P is the intervening portion (which takes it from S_k to S_k). Q is denoted by $\alpha_{ik}{}^{k-1}$, R by $\alpha_{kj}{}^{k-1}$ and P by $(\alpha_{kk}{}^{k-1})^*$. Hence QPR is denoted by $\alpha_{ij}{}^k$ as constructed.

This proves that $\alpha_{ij}{}^k$ denotes all the sequences satisfying the construction. Using the inductive hypothesis, one can easily see that it satisfies only such sequences.

Theorem 2.2. If an automaton is described by a state graph with states $S_1, \cdots, S_n$ whose initial state is S_i and whose states of output 1 are $S_{u_1}, \cdots, S_{u_m}$, then the automaton is described by the regular expression

$$\alpha_{iu_1}{}^n \cup \cdots \cup \alpha_{iu_m}{}^n.$$

This theorem is a direct consequence of theorem 2.1. Note that if the state graph of an automaton has no states of output 1 then Λ describes the automaton. Otherwise a regular expression is given by theorem 2.2. Thus, every automaton is described by some regular expression.

Although the method of construction is somewhat complicated, we have found no more direct general method for converting a state graph to a regular expression. Part of the problem is that it is rather difficult to get a regular expression denoting the input sequences of all paths from S_i to S_j, since these may involve many loops.

To obtain a regular expression from a state graph, one must first assign an order to the states. Different orderings will, in general, result in different regular expressions. One should attempt to order the states so that the simplest regular expression results. One strategic consideration is that those states bearing the most traffic (those with the largest number of arrows pointing to them) should come later in the ordering.

If we count the number of digits in a regular expression as its size, then the maximum size of $\alpha_{ij}{}^k$ is $2 \cdot 4^k$. A reduced n-state graph has a maximum of $n-1$ states with output 1. (If all n states had output 1 then the graph would reduce to a one-state graph.) Hence, the maximum size of a regular expression constructed from an n-state graph is $(n-1)2 \cdot 4^n$. Actually it will usually be much less than this, because simplifications can often

e made along the way, as when $i=k$ or $j=k$. Thus $\alpha_{ij}{}^{i}$ by construction

$$\alpha_{ij}{}^{i-1} \cup \alpha_{ii}{}^{i-1}(\alpha_{ii}{}^{i-1})^*\alpha_{ij}{}^{i-1},$$

hich reduces to

$$(\alpha_{ii}{}^{i-1})^*\alpha_{ij}{}^{i-1}.$$

ikewise $\alpha_{ij}{}^{j}$ reduces to

$$\alpha_{ij}{}^{j-1}(\alpha_{jj}{}^{j-1})^*.$$

Iowever, the size of the regular expression, though generally much less than $(n-1)2\cdot 4^n$, is still rather large. Ve are of the opinion that the simplest regular expression describing an automaton is usually quite large in omparison to the simplest state graph.

As an example, consider the state graph of Fig. 3. A egular expression for it is $\alpha_{21}{}^{3}$. We find that

$$\alpha_{21}{}^{2} = (10)^*1,$$
$$\alpha_{23}{}^{2} = (10)^*(11 \cup 0),$$
$$\alpha_{33}{}^{2} = 0 \cup 1(10)^*(11 \cup 0),$$
$$\alpha_{31}{}^{2} = 1(10)^*1.$$

It is an easy matter to obtain these by inspection from he state graph. Alternatively they can be obtained by neans of the algorithm, making use of simplifications ased on laws developed in section I.) Thus,

$$\alpha_{21}{}^{3}$$
$$= (10)^*1 \cup (10)^*(11 \cup 0)[0 \cup 1(10)^*(11 \cup 0)]^*1(10)^*1.$$

On the other hand, if the states are labeled as in Fig. , the desired regular expression is $\alpha_{31}{}^{3}$. We find that

$$\alpha_{33}{}^{2} = 10 \cup (0 \cup 11)0^*1,$$
$$\alpha_{31}{}^{2} = 1,$$

nd therefore,

$$\alpha_{31}{}^{3} = [10 \cup (0 \cup 11)0^*1]^*1.$$

Although this regular expression and the one obtained previously describe the same automaton and are equivaent, this equivalence is far from obvious.

III. An Algorithm for Constructing a State Graph of an Automaton from a Restricted Regular Expression

A restricted regular expression is one which has no cap, tilde, phi, or lambda. Associate with each occurence of a digit in a restricted regular expression a *position*, which can best be regarded as being directly to the right of the digit. Then in generating a sequence denoted by a regular expression one can think of going from position to position, through the digit of the latter position. For example, consider the restricted regular

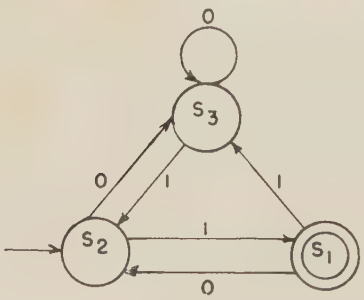

Fig. 3.

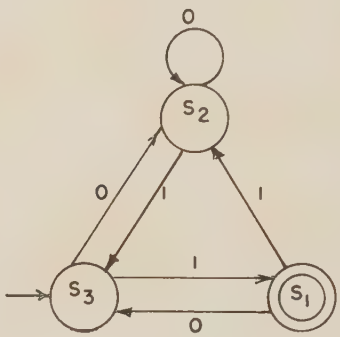

Fig. 4.

expression $((0\cdot 0 \cup 1\cdot 1)^*0\cdot 1)^*$. There are six positions in this expression. From left to right let these be 0_1 (the position to the right of the first zero), 0_2, 1_1, 1_2, 0_3, and 1_3. An alternative formulation of the notion of a sequence denoted by a restricted regular expression can be given in terms of these positions.

In the definitions that follow, restricted regular expressions that denote the empty sequence are distinguished from those that do not. The following recursive characterization of this property for the general class of regular expressions is given, because of its usefulness in the next section as well as in this section. 1) ϕ denotes the empty sequence, but Λ, 0, 1 do not. 2) For every α, α^* denotes the empty sequence. 3) For every α, $\sim\alpha$ denotes the empty sequence if and only if α does not. 4) $\alpha_1 \cup \cdots \cup \alpha_n$ denotes the empty sequence if and only if at least one α_i does. 5) $\alpha_1\alpha_2 \cdots \alpha_n$ denotes the empty sequence if and only if every α_i does. 6) $\alpha_1 \cap \alpha_2 \cap \cdots \cap \alpha_n$ denotes the empty sequence if and only if every α_i does.

For the purposes of this section, we do not have to refer to 3) and 6) of this definition. It is worthwhile to note that no restricted regular expression without a star denotes the empty sequence.

Let α be a well-formed part of a restricted regular expression ρ. Then "terminal position of α" is defined recursively as follows: 1) If α has only a single position then that position is a terminal position of α. 2) If α is $\beta_1 \cup \beta_2 \cup \cdots \cup \beta_n$ then any terminal position of any of the β's is a terminal position of α. 3) A terminal position

of β is a terminal position of β^*. 4) If α is $\beta_1 \cdot \beta_2 \cdot \cdots \cdot \beta_n \cdot$ and if for every x, $n \geqq x > j$, β_x denotes the empty sequence, then a terminal position of β_j is a terminal position of α; in particular, a terminal position of β_n is a terminal position of α. 5) No position is a terminal position of α unless its being so follows from 1), 2), 3), and 4).

"Initial position of α" is defined recursively as follows: 1) If α has only a single position then that position is an initial position of α. 2) If α is $\beta_1 \cup \cdots \cup \beta_n$ then an initial position of any of the β's is an initial position of α. 3) An initial position of β is an initial position of β^*. 4) If α is $\beta_1 \cdot \beta_2 \cdot \cdots \cdot \beta_n$ and for all x, $1 \leqq x < j$, β_x denotes the empty sequence, then an initial position of β_j is an initial position of α. (Thus, in any case, an initial position of β_1 is an initial position of α.) 5) Nothing is an initial position of α unless its being so follows from 1), 2), 3), and 4).

It can be proved that the left-most position of α is always an initial position of α, and likewise that the right-most position of α is a terminal position of α, although these are not always the only initial and terminal positions. For example, in $(0_1 \cup 1_1)^* 0_2 0_3$, 0_2 and 1_1 as well as 0_1 are initial positions, although 0_3 is the only terminal position.

A transition of a restricted regular expression ρ is an ordered pair of positions $\langle P_1 P_2 \rangle$ such that, either P_1 is a terminal position of α, P_2 is an initial position of β, and $\gamma_1 \cdot \cdots \cdot \gamma_m \cdot \alpha \cdot \delta_1 \cdot \cdots \cdot \delta_n \cdot \beta \cdot \eta_1 \cdot \cdots \cdot \eta_q$ ($m \geqq 0$, $n \geqq 0$, $q \geqq 0$) is a well-formed part of ρ where each of the δ's denotes the empty sequence, or P_1 is a terminal position of α^* and P_2 is an initial position of α^*, where α^* is a well-formed part of ρ.

An allowable sequence of positions of ρ is a finite sequence of positions $P_1, \cdots, P_n$ of ρ such that P_1 is an initial position of ρ, P_n is a terminal position of ρ and, for each $i < n$, $\langle P_i P_{i+1} \rangle$ is a transition of ρ.

Theorem 3.1. A finite sequence S of 0's and 1's is denoted by a restricted regular expression ρ if and only if there exists an allowable sequence R of positions of ρ such that S results from R by replacing each position by the digit of that position.

This theorem follows from the above definitions and the definition of denotation given in section I. (A rigorous proof would be by induction, following the recursive definition of "regular expression," restricted. We trust that the construction of this proof would be an easy task for the interested reader.)

If a restricted regular expression ρ containing p positions describes the behavior of an automaton, a state graph containing 2^p+1 states can be constructed by the method given below. It will be proved that this state graph is a state graph for the given automaton. (In practice, usually a far simpler state graph will suffice. It will turn out that many of the 2^p+1 states will not be used.)

Construction method. Let ρ have p positions. Then let there be an initial state, and, in addition, one state for each set of positions (thus giving 2^p+1 states). An input of 0 applied to a state corresponding to a set S of positions will lead to the state corresponding to the set S' of just those positions P such that P's digit is 0 and there is a transition from at least one position of S to P. The same statement applies for an input of 1. If there is no such position P then the preceding sentence implies that it leads to the state corresponding to the null set of positions; also implied is that an input applied to the state corresponding to the null set results again in that state. An input of 0 applied to the initial state results in the set of all positions P which are initial positions of ρ and whose digit is 0. The same statement applies for an input of 1. A state has an output of 1 if and only if there is at least one position in the corresponding set of positions which is a terminal position of ρ.

In discussing this construction method we shall verbally identify a state of the resulting state graph with the corresponding set of positions.

Theorem 3.2. The state graph G obtained from ρ by the above construction method describes the behavior of the same automaton as ρ.

By theorem 3.1, it is sufficient to prove, for any sequence of inputs $i_1, \cdots, i_n$ that takes the state graph from the initial state through a series of states $S_1, \cdots, S_n$, that S_n is a state of output 1 if and only if there exists an allowable sequence of positions $P_1, \cdots, P_n$ such that for each j, $1 \leqq j \leqq n$, i_j is the digit of P_j.

Lemma. For each S_j of the sequence $S_1, \cdots, S_n$, all positions of S_j have the same digit, namely i_j.

The proof is immediate from the construction. (This lemma shows that many of the 2^p+1 states are dispensable in the state graph, namely, those states some of whose positions have the digit 0 and others have 1. Usually, many states other than those shown to be dispensable by this lemma are also dispensable.)

To proceed with the proof of theorem 3.2, suppose first that S_n is a state of output 1. Then, by construction, there exists a position P_n in S_n such that P_n is terminal in ρ. There must exist a position P_{n-1} of S_{n-1} such that $\langle P_{n-1} P_n \rangle$ is a transition of ρ; otherwise P_n would not be in S_n, by construction. Likewise there must be a P_{n-2} in S_{n-2} such that $\langle P_{n-2} P_{n-1} \rangle$ is a transition of ρ. And so on, back. The resulting sequence of positions $P_1, \cdots, P_n$ is an allowable sequence of positions of ρ, since P_1 is an initial position of ρ (for, by construction, S_1 is the set of initial positions of ρ having the digit i_1), for every $j < n$ $\langle P_j P_{j+1} \rangle$ is a transition of ρ, and P_n is a terminal position of ρ. Furthermore, by the lemma, for each j, i_j is the digit of P_j. This concludes one direction of the proof of theorem 3.2.

To prove theorem 3.2 the other way, suppose that there exists an allowable sequence of positions $P_1, \cdots, P_n$ such that, for each $j \leqq n$, i_j is the digit of P_j. By con-

truction, S_1 must be the set of initial positions with i_1 as digit, including P_1. S_2 must have P_2 as a member, since $\langle P_1 P_2 \rangle$ is a transition of ρ. Likewise S_3 must have P_3 as a member, and so on. Thus S_n must have P_n as a member and therefore must be a state of output 1. This completes the proof of theorem 3.2.

We close this section with a practical method of obtaining the state graph from a restricted regular expression. Far fewer states than 2^p+1 are usually needed, so it is not expedient to assume this many states at the beginning. Rather the method constructs the state graph state by state, adding states only when they are needed. The method will be explained by means of a short example.

Let ρ be $1(00 \cup 01)^*0$. There are six positions which are in order $1_1, 0_1, 0_2, 0_3, 1_2, 0_4$. Rewriting ρ with positions for digits we get $1_1(0_1 0_2 \cup 0_3 1_2)^* 0_4$. 1_1 is the only initial position of ρ. 0_4 is the only terminal position of ρ. The transitions are

$$\langle 1_1 0_1 \rangle, \quad \langle 1_1 0_3 \rangle, \quad \langle 1_1 0_4 \rangle$$
$$\langle 0_1 0_2 \rangle$$
$$\langle 0_3 1_2 \rangle$$
$$\langle 0_2 0_1 \rangle, \quad \langle 0_2 0_3 \rangle, \quad \langle 0_2 0_4 \rangle$$
$$\langle 1_2 0_1 \rangle, \quad \langle 1_2 0_3 \rangle, \quad \langle 1_2 0_4 \rangle.$$

In constructing the state graph we first assume the initial state. We then ask, what state, *i.e.*, set of positions, do we get to by an initial input of 1 and what state do we get to by an initial input of 0? An input of 1 applied to the initial state I lands us in state $\{1_1\}$, whose only position is 1_1. An input of 0 applied to I lands us in the state Λ, corresponding to the null set of positions. Once in this state the automaton can never get out of it, so a descriptive name for it is "the dead state." An input of 0 applied to $\{1_1\}$ results in the state $\{0_1, 0_3, 0_4\}$; an input of 1 results in Λ. An input of 0 applied to $\{0_1, 0_3, 0_4\}$ results in the state $\{0_2\}$; an input of 1 results in the state $\{1_2\}$. An input of 1 applied to $\{0_2\}$ results in Λ; an input of 0 results in $\{0_1, 0_3, 0_4\}$. The same is true of inputs applied to $\{1_2\}$. These then are all the states that are needed. $\{0_1, 0_3, 0_4\}$ is the only state which has an output of 1. The completed state graph is therefore as in Fig. 5. Thus 6, and not 33, states result. The reduced state graph of this graph (see Moore[1]), by which the states $\{1_1\}$, $\{1_2\}$ and $\{0_2\}$ all collapse into a single state, has only 4 states!

IV. Complementation and Intersection in Regular Expressions

Because it is convenient to allow complementation and intersection in regular expressions that specify the behavior of automata, we extend the method of the previous section to the general class of regular expressions.

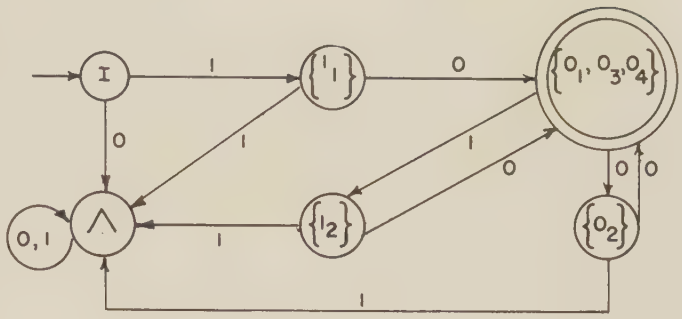

Fig. 5.

Assume that ϕ and Λ do not occur in the regular expression, since they can be eliminated by the following rules:

$$\phi = \sim((0 \cup 1)(0 \cup 1)^*),$$
$$\Lambda = \sim((0 \cup 1)^*).$$

Actually, simplicity will often result by using the equations given at the end of section I wherever possible in eliminating ϕ and Λ; for example,

$$\alpha\Lambda = \Lambda.$$

Note first that if an expression has the tilde or cap in it, it is not possible to extend the method of section III in the obvious fashion. If a regular expression contains only cups, stars, and dots, at each digit of a sequence of 0's and 1's we can think of ourselves as being in any one of a set of positions of the regular expression. This seems to be no longer possible if the regular expression contains intersection or complementation.

The method for regular expressions containing a tilde or cap is roughly as follows. Suppose first that only a single tilde and no cap occurs in ρ, and that $\sim\alpha$ is a well formed part of ρ. A state graph for α is made into a state graph for $\sim\alpha$; then these states are used as positions along with the positions of the digits outside of $\sim\alpha$ in ρ in obtaining the state graph for ρ. If ρ contains a single cap and no tilde and $\alpha \cap \beta$ is a well formed part of ρ, then a state graph is obtained for $\alpha \cap \beta$ by a modification of the method of section III; using these states as positions as well as the digits of ρ outside $\alpha \cap \beta$, a state graph is obtained for ρ. If ρ contains several tildes or several caps or both tildes and caps, then the above steps must be repeated in the appropriate order. For example, if ρ is $\alpha \cdot ((\sim\beta \cdot \sim\gamma)^* \cap \delta)$ where α, β, γ, and δ contain no caps or tildes, then in order to obtain a state graph for ρ, state graphs G_1 and G_2 are first obtained for $\sim\beta$ and $\sim\gamma$ respectively. Using states of G_1 and G_2 as positions, a state graph G_3 for $(\sim\beta \cdot \sim\gamma)^*$ is obtained. From G_3 and a state graph for δ, a state graph G_4 for $(\sim\beta \cdot \sim\gamma)^* \cap \delta$ is obtained. Then using the states of G_4 and the digits of α as positions, a state graph G is obtained for ρ.

Theorem 4.1. If G is a state graph for α and G' results from G by reversing the output of every state of G from 0 to 1 or from 1 to 0, then G' is a state graph for $\sim\alpha$.

Proof: A sequence S is denoted by $\sim\alpha$ if and only if S is not denoted by α, which is so if and only if S applied to G results in output 0, which is so if and only if S applied to G' results in output 1. Q.E.D.

Theorem 4.2. Let G_1 and G_2 be state graphs for α and β, respectively. Let G be the state graph whose states are $\langle g_1g_2\rangle$ for all g_1 in G_1 and g_2 in G_2, such that there is a transition in G from $\langle g_1g_2\rangle$ to $\langle g_1'g_2'\rangle$ under input i if and only if there is a transition in G_1 from g_1 to g_1' under input i and a transition in G_2 from g_2 to g_2' under input i, such that the initial state of G is the state $\langle I_1I_2\rangle$ where I_1 and I_2 are the initial states of G_1 and G_2 respectively, and such that $\langle g_1g_2\rangle$ has output 1 in G if and only if g_1 has output 1 in G_1 and g_2 has output 1 in G_2. Then G is a state graph for $\alpha\cap\beta$.

Proof: A sequence S is denoted by $\alpha\cap\beta$ if and only if it is both denoted by α and denoted by β, which is so if and only if when S is applied to G_1 it yields an output 1 and when S is applied to G_2 it yields an output 1, which is so if and only if when S is applied to G there is an output 1 (which can be seen from the construction explicit in the statement of the Theorem). Q.E.D.

A state graph is *input-pure* if no two of its transitions leading into the same state have different inputs. For state graphs that are not input-pure, there is a simple method of constructing an equivalent input-pure state graph. For example, the state graph of Fig. 6, which is not input-pure can, by dividing S_3 into S_3' and S_3'', be converted into the equivalent state graph of Fig. 7, which is input-pure.

Let $\alpha_1, \cdots, \alpha_r$ be well-formed parts of ρ such that no α_i is a part of any other α_j, and such that no tilde or cap appears in ρ outside of the α's. For each i let G_i be an input-pure state graph for α_i. Then let the positions of ρ (with respect to $\alpha_1, \cdots, \alpha_r, G_1, \cdots, G_r$) be the digits of ρ outside of the α's and the states of $G_1, \cdots, G_r$. The digit of the latter type of position is the input on all the transitions leading to the state in the state graph. We must redefine some of the concepts introduced in section III.

A state g_i is an *initial* position of α_i if and only if there is a transition from the initial state of G_i to g_i in G_i. (Note that the initial state of G_i is not necessarily an initial position of α_i.) A state g_i of G_i is a *terminal* position of α_i if and only if g_i is a state of output 1 of G_i. From here on the definition of "initial" and "terminal" are the same as in section III. Well formed proper parts of the α's do not have initial and terminal positions, under the new definition, but all other well formed parts of ρ do.

$\langle P_1P_2\rangle$ is a transition of ρ (with respect to $\alpha_1, \cdots, \alpha_r, G_1, \cdots, G_r$) if and only if either 1) P_1 and P_2 are states of the same G_i and there is a transition in G_i from P_1 to P_2, or 2) P_1 and P_2 are not states of the same G_i and

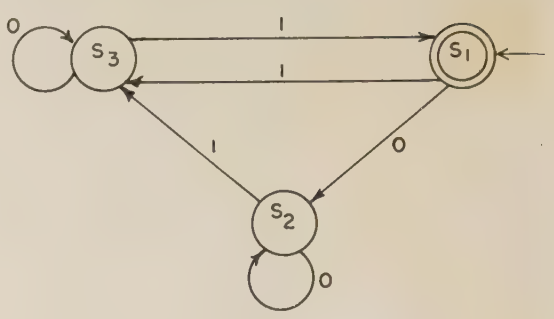

Fig. 6.

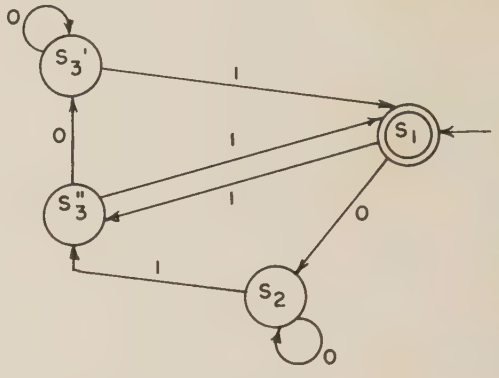

Fig. 7.

$\langle P_1P_2\rangle$ is a transition according to the definition of section III. An *allowable sequence of positions* of ρ (with respect to $\alpha_1, \cdots, \alpha_r, G_1, \cdots, G_r$) is a finite sequence of positions (with respect to $\alpha_1, \cdots, \alpha_r, G_1, \cdots, G_r$), $P_1, \cdots, P_n$, such that P_1 is an initial position of ρ, P_n is a terminal position of ρ and, for each $i<n$, $\langle P_iP_{i+1}\rangle$ is a transition of ρ. (This definition is the same, word for word, as that of section III, and the following theorem is almost the same as theorem 3.1.)

Theorem 4.3. If no tildes, caps, phis, or lambdas occur outside $\alpha_1, \cdots, \alpha_r$ in ρ, and if $G_1, \cdots, G_r$ are input-pure state graphs for $\alpha_1, \cdots, \alpha_r$, respectively, then a finite sequence S of 0's and 1's is denoted by a regular expression ρ if and only if there exists an allowable sequence R of positions for ρ (with respect to $\alpha_1, \cdots, \alpha_r, G_1, \cdots, G_r$), such that S results from R by replacing each position by the digit of that position.

The proof follows from the definitions. (As in the case of theorem 3.1 we allow the interested reader to construct the rigorous proof for himself.)

We close with an example. Let ρ be $0\sim[1(00\cup01)^*0]11$. Let β be $[1(00\cup01)^*0]$, and let α be $\sim\beta$. Then β is the ρ of the example at the end of section III. A state graph for β (obtained from the one of section III by reduction) is shown in Fig. 8. By converting single circles into double circles and vice versa, we obtain a state graph for α, which is then converted into the input-pure state graph G of Fig. 9. The positions of ρ with respect to α and G are 0_1, A, D_0, D_1, B_1, C, B_0, 1_1 and 1_2. (0_1, 1_1 and 1_2, of course, refer to positions of ρ outside α.) The initial positions of α are D_0 and B_1; the terminal posi-

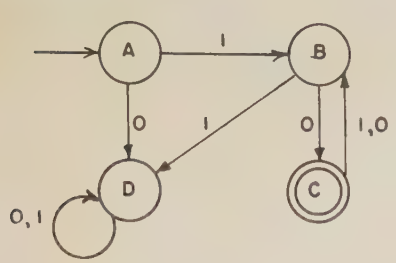

Fig. 8.

ions of α are all the states of G except C. The transitions of ρ are then

$$\langle 0_1 B_1 \rangle, \qquad \langle 0_1 D_0 \rangle$$
$$\langle A 1_1 \rangle$$
$$\langle B_1 1_1 \rangle$$
$$\langle B_0 1_1 \rangle$$
$$\langle D_0 1_1 \rangle$$
$$\langle D_1 1_1 \rangle$$
$$\langle 1_1 1_2 \rangle,$$

and those shown on the state graph. Using the procedure of section III, we obtain the state graph of Fig. 10 for ρ. Note that the position A does not appear. In general the initial state s of G will not be used in obtaining the state graph for ρ if there is no transition into s in G, unless s is also an initial position in ρ. By the process of reduction, $\{B_0\}$ and $\{B_1\}$ collapse into a single state.

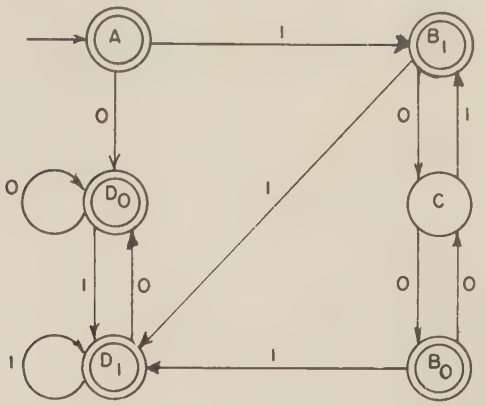

Fig. 9.

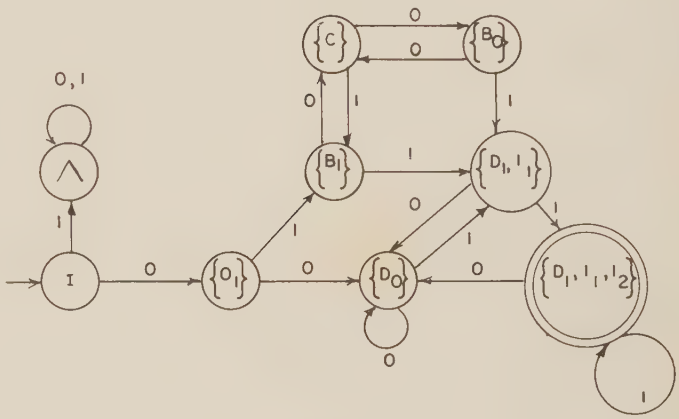

Fig. 10.

A Method for the Design of Pattern Recognition Logic*

SAM D. STEARNS†

Summary—The general problem of pattern recognition is regarded as a problem wherein the recognition device is presented with a plane array of black-or-white elements and must decide to which general class (pattern) this array belongs.

A method for reducing the necessary amount of logic is presented. It is basically a method for reducing Boolean equations in many variables which contain large numbers of redundant or "don't care" terms.

The reduced logic is in the form of Boolean functions of the black-or-white elements. Some experimental results, in which this logic was mechanized with diodes, are discussed.

Introduction

A FAIRLY general approach to the problem of pattern recognition may be taken by making the following assumptions at the outset:[1]

1) The pattern to be recognized always may be made to occupy a fixed, finite, rectangular area on a plane.
2) This area may be divided into n elements.
3) Each element may be designated either black or white.

This "binary quantization" of the pattern on a plane allows one to make the following definitions:

Pattern field—the area referred to above, divided into n subareas, called *elements*.

State of an element—1 if it is black; 0 if it is white.

Image—any specified set of states of the n elements. (For a given pattern field, there are 2^n possible images.)

Pattern—any specified set of images. (A pattern may either include or not include a given image. Hence, there are $(2)^{2^n}$ different patterns.)

These definitions are illustrated in Fig. 1.

Using the above terminology, the problem of pattern recognition seems to involve four basic steps.

1) Designate the entire set of patterns which must be recognized (distinguished from one another), *e.g.*, the integers from 0 through 9, or the Greek alphabet, or the footprints of 10 different animals, etc.
2) Choose a number of elements (n) which is at least large enough to make the patterns mutually exclusive, *i.e.*, so that no pattern includes an image that is included in another pattern.

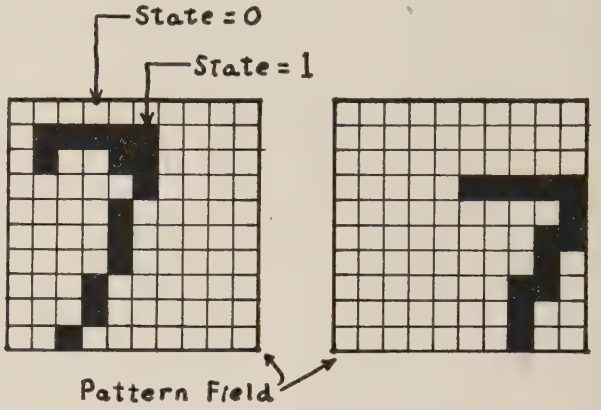

Fig. 1—Two different images of the same pattern; $n = 100$.

3) Determine some or all of the different images which are included in each of the patterns.
4) Determine a logical structure which, when presented with the n binary inputs representing the states of the n elements, will indicate a specific pattern.

Step 1) above is accomplished by the designer, who chooses a set of patterns for the application which he has in mind. Step 2) would usually be accomplished by experimental or empirical means. The designer could probably increase the number of elements (n) until he was certain that his patterns were mutually exclusive. Step 3) is a difficult problem in many cases. It could possibly be accomplished analytically, by considering images of various sizes and in various orientations, positions, etc.; or it could be accomplished by observing and recording the various images of each pattern. Step 4) is another very difficult problem, and the remainder of this paper is a discussion of it, along with one solution and pertinent experimental results.

Boolean Representation of the Logic Problem

Using the above definitions of pattern, image, etc., it is easy to state the basic necessities of the recognition logic in terms of Boolean algebra. Let the elements of the pattern field be designated

$$e_1, e_2, e_3, \cdots, e_n,$$

as shown in Fig. 2. Then a particular image could be represented in Boolean algebra by the product

$$\prod_{i=1}^{n} e_i^{(a_i)},$$

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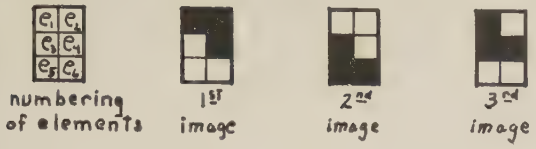
† Sandia Corporation, Albuquerque, N. M.

[1] These assumptions may, in some cases, be too severe. For example, they would not be reasonable in the case of cursive handwriting.



$$P = {}^{1\,1\,0\,1\,0\,0}e_1e_2e_3e_4e_5e_6 + {}^{0\,0\,1\,0\,1\,1}e_1e_2e_3e_4e_5e_6 + {}^{1\,0\,1\,1\,0\,0}e_1e_2e_3e_4e_5e_6$$

Fig. 2—Boolean representation of a pattern.

here q_i is the state of e_i and indicates negation if the ement is white. A pattern would then be the Boolean m of all of its included images, or

$$P_k = \sum_{j=1}^{I} \prod_{i=1}^{n} e_i^{(q_{ijk})} \tag{1}$$

here there are a total of I images and the subscript j esignates a particular image (see Fig. 2). Eq. (1) is said be in "canonical" form, because each product-term ntains every variable.

Thus, the entire recognition logic may be represented a set of equations of the form

$$\begin{aligned} P_1 &= \sum_{j=1}^{I_1} \prod_{i=1}^{n} e_i^{(q_{ij1})}, \\ P_2 &= \sum_{j=1}^{I_2} \prod_{i=1}^{n} e_i^{(q_{ij2})}, \\ &\vdots \\ P_p &= \sum_{j=1}^{I_p} \prod_{i=1}^{n} e_i^{(q_{ijp})}. \end{aligned} \tag{2}$$

he input variables to the logic would be $e_1, e_2, \cdots, e_n$, nd the output variables would, of course, be $_1, P_2, \cdots, P_p$ where p is the total number of patterns be recognized.

In the experimental device which will be described ter, a value of 150 was chosen for n. Thus, the equaons in (2), in their present form, would in general be oo long even to write out, let alone mechanize (each m could contain up to 2^{150}, or about 10^{45} products).

These equations must be reduced, but again they are general too complex to be reduced by any of the nown techniques for Boolean minimization.[2] Before scussing a method of reduction, however, we can comine these equations in such a manner that the outputs the logic are coded representations of $P_1, P_2, \cdots, P_p$ lthough this is not necessary to the reduction method self). An example will serve to illustrate this.

Suppose that the patterns to be recognized consist eight types of blood cells, designated $P_1, P_2, \cdots, P_8$. et the logic have only 3 outputs instead of 8, and let ese be O_1, O_2, and O_3. The "output truth table" could en be as in Table I.

TABLE I
BINARY-CODED-DECIMAL REPRESENTATION OF PATTERNS

	O_1	O_2	O_3
P_1	0	0	0
P_2	0	0	1
P_3	0	1	0
P_4	0	1	1
P_5	1	0	0
P_6	1	0	1
P_7	1	1	0
P_8	1	1	1

In the above example, the recognition logic would be represented by the following equations:

$$\begin{aligned} O_1 &= P_5 + P_6 + P_7 + P_8, \\ O_2 &= P_3 + P_4 + P_7 + P_8, \\ O_3 &= P_2 + P_4 + P_6 + P_8. \end{aligned} \tag{3}$$

Substituting (2) into (3) results in

$$\begin{aligned} O_1 &= \sum_{k=5,6,7,8} \sum_{j=1}^{I_k} \prod_{i=1}^{n} e_i^{(q_{ijk})}, \\ O_2 &= \sum_{k=3,4,7,8} \sum_{j=1}^{I_k} \prod_{i=1}^{n} e_i^{(q_{ijk})}, \\ O_3 &= \sum_{k=2,4,6,8} \sum_{j=1}^{I_k} \prod_{i=1}^{n} e_i^{(q_{ijk})}. \end{aligned} \tag{4}$$

An example of these equations is given in the Appendix. When these equations are reduced, there will clearly be more terms capable of being combined in each equation than there are in the equations in (2), since here there are the same number of product-terms in three equations instead of eight. Furthermore, even more term-combining may be anticipated if patterns which are topologically similar to each other are made to correspond to the output groups (P_5, P_6, P_7, P_8), (P_3, P_4, P_7, P_8), and (P_2, P_4, P_6, P_8).

The Method of Classifiers[3]

The output equations in the form of the equations in (4) are said to be in canonical form, because as in (1), each of the product-terms of each equation contains every variable. It was mentioned that each product-term represents a particular image. In general, most of the images (canonical terms) do not occur as product-

[2] See, for example, M. Phister, Jr., "Logical Design of Digital omputers," John Wiley and Sons, Inc., New York, N. Y., pp. 61–9; 1959.

[3] Developed in cooperation with D. R. Morrison, Sandia Corp., Albuquerque, New Mex.

terms in any of the output equations, because, in general, the number of images which belong to specified patterns is a very small percentage of the total number (2^n) of images. All of the images which do not occur as product-terms in any of the output equations may be considered as redundant, or "don't-care," terms when the output equations are reduced. If the number of these images is large, they may be used effectively in reducing the output equations.

To make use of these redundant images, we first define an operation, S, on a sequence of one or more Boolean products. This operation has the effect of forming a single new product which contains only those elements which have the same exponent (are in the same state) in all of the original products. For example,

$$S(\overset{1\,1\,1\,0}{e_1e_2e_3e_4},\quad \overset{1\,0\,0\,0}{e_1e_2e_3e_4},\quad \overset{1\,1\,0\,0}{e_1e_2e_3e_4}) = \overset{1\,0}{e_1e_4}.$$

Only e_1 and e_4 have the same exponents in all three terms. The pictorial analogy of this operation is shown in Fig. 3. The three original images are combined, under the operation S, into a single array in which only the states of elements e_1 and e_4 are specified, the remaining elements being "gray" (either black or white).

It is noted in passing that, if image

$$I_j = \prod_{i=1}^{n} e_i^{(q_{ij})},$$

then $S(I_j) = I_j$; and further, that $S(I_j,\ I_k) = S(I_k,\ I_j)$. Also, the following convention is adopted:

$$S\left(I_j, \sum_{k=1}^{t} I_k\right) = \sum_{k=1}^{t} S(I_j, I_k).$$

Now consider the output equations in (4). Perform the operation

$$S\left[\prod_{i=1}^{n} e_i^{(q_{i15})}, \prod_{i=1}^{n} e_i^{(q_{i25})}\right] \tag{5}$$

on the first two images of output O_1. Then perform the operation

$$S\left\{S\left[\prod_{i=1}^{n} e_i^{(q_{i15})}, \prod_{i=1}^{n} e_i^{(q_{i25})}\right], \left[\sum_{k=1,2,3,4} \sum_{j=1}^{I_k} \prod_{i=1}^{n} e_i^{(q_{ijk})}\right]\right\}. \tag{6}$$

Operation (6) will result in a Boolean sum of many terms. Now make the following test: "Is the number of variables in the result of operation (5) greater than the number of variables in *every term* of the sum which results from (6)?" If the answer is "yes," then the term resulting from (5) may be called a *classifier* for the two images in (5), because the term resulting from (5) contains the necessary information for specifying to which of the three outputs the two images in (5) belong. If the answer is "no," then other combinations of images may be tried in (5), and the results tested in (6).

If the classifier resulting from (5) is used to replace the two terms of (5) in the first of the equations in (4), then clearly there will be one less product-term to mechanize in (4), and also, one product-term will consist of fewer than n elements. Hence, this process of forming classifiers is a process for reducing equations like (4). Note that some of the "redundant images" mentioned previously are utilized implicitly whenever a classifier is formed.

Fig. 3—Pictorial representation of the operation S.

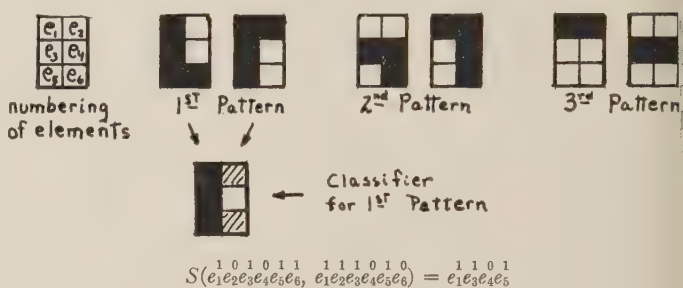


Fig. 4—Forming a classifier.

In Fig. 4, a pictorial example of a classifier is shown. The classifier is shown for two images of the first pattern, and it is equivalent to

$$S[\overset{1\,0\,1\,0\,1\,1}{e_1e_2e_3e_4e_5e_6},\ \overset{1\,1\,1\,0\,1\,0}{e_1e_2e_3e_4e_5e_6}] = \overset{1\,1\,0\,1}{e_1e_3e_4e_5}.$$

The gray elements in the classifier contain no information; the black and white elements alone are capable of distinguishing as to which pattern the two images belong.

When confronted with a set of output equations like (4), one must decide on how to choose the sets of images on which operations (5) and (6) are performed. This decision will depend on how much computing time can be expended and on how much reduction is necessary in the output equations. Fig. 6 is a flow chart which exhibits one method for choosing images on which to try operations (5) and (6). In the Appendix, an example is given in which a particular set of output equations as in (4) is processed by the method of Fig. 6 to form a set of classifiers for, and thus reduce, the first of the equations in (4).

Experimental Results

Several experiments have been performed along the es described above, and, to some degree, the recog- ion of typewritten and handwritten figures and char- ers has been achieved. To determine the various ages, or product-terms in the output equations, the ording system shown in Fig. 5 was employed.

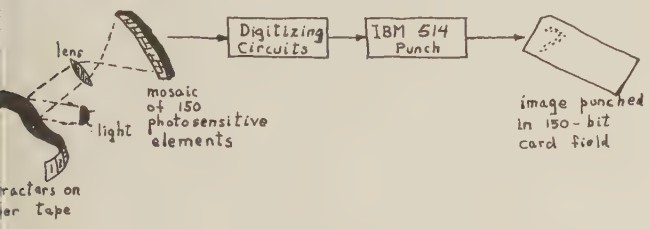


Fig. 5—Pattern recording system.

The use of a mosaic of photoconductive cells instead the usually-employed scanning equipment seemed ite satisfactory. The patterns were written in framed eas on paper tape, and automatically passed under the s by means of a paper tape reader. The usual pro- lure was to have people draw the same pattern re- atedly in the framed areas along the paper tape, and en to punch these images, one to a card. After some rds have been thrown out so that, in the ones that re- in, no two images are exactly alike, one has a set of oduct-terms in the output equations in the form (4).

To form groups of output equations, several different ts of patterns were chosen in different experiments. ypes of patterns included alphabetic and numeric aracters, and simple figures such as squares, triangles, cles, etc.

Using the IBM 704 computer with an 8192-word core emory, the process shown in Fig. 6 was followed, re- lting in a set of classifiers. (An example using this ocess is given in the Appendix.) The process used was, course, only one of many possibilities; furthermore, allows the computer to discover only a very small per- ntage of all of the possible classifiers. However, this ocess resulted in considerable reduction of the output uations.

In one experiment, images were obtained for the ten pewritten digits. After about 100 unique images for ch digit had been recorded, the equations

$$O_1 = D_3 + D_8 + D_9 + D_5 + D_4 + D_2 + D_7 + D_1,$$
$$O_2 = D_3 + D_8 + D_9 + D_5 + D_0 + D_6,$$
$$O_3 = D_3 + D_8 + D_4 + D_2 + D_0 + D_6,$$
$$O_4 = D_3 + D_9 + D_4 + D_7 + D_0, \qquad (7)$$

here D_i is the ith digit from 0 through 9, were reduced y the method of Fig. 6. (There is no outstanding reason r this particular choice of code.) In all of our experiments, a 150-element pattern field was used. Hence, the equations in (7), before reduction, each consisted of several hundred products, each product containing 150 elements. After reduction, the functions for O_1 through O_4 were each sums of 5 or fewer products, and each product consisted of only 2 or 3 elements. When mechanized with diode logic, the reduced functions achieved recognition of about 99 per cent of all typewritten images "read in." This was due in part to the fact that the images of each pattern were quite similar to each other, plus the fact that the equations in (7) contained, as stated, a rather large number of product-terms. Also, it should be mentioned that the typewritten characters from which the images were taken were quite clean, and that the area surrounding the characters contained very little "noise."

The method of Fig. 6 seems to have a sort of built-in feature of extracting, from large numbers of images, the important or invariant qualities of the patterns. For example, in an experiment with three different handwritten figures (squares, triangles, and crosses), the classifiers were mechanized with diode logic and were then capable of recognizing a variety of new images, none of which had been used to form the classifiers.

Further Considerations

With handwritten characters, as would be expected, a very large number of unique images must be recorded in order to achieve adequate recognition of the characters after the classifiers are found. Also, the number of classifiers for a group of handwritten patterns is, of course, much larger than the number of classifiers for the same group of typewritten patterns. One rather general way to reduce both the required number of unique images and the number of classifiers is to perform one or more transformations, or mappings, on the original pattern field. As shown in Fig. 7, these mappings should occur in such a manner that each of the 2^n images is mapped to a point in a new set of less than 2^n points, and also such that images of the same pattern tend to converge onto the same points, thus decreasing the number of terms in the output equations when they are written in the form of (4).

An obvious example of such a mapping is the transformation which causes any figure appearing on the pattern field to be shifted so that its centroid lies directly at the center of the pattern field. Clearly, this particular mapping causes images of the same pattern to converge into the same image.

Another simple mapping is the autocorrelation of an image. This also causes image-conversion within a pattern, primarily because the autocorrelation function is the same for the same figure appearing in two different positions in the pattern field.

We are presently evaluating different mapping schemes in order to determine their effectiveness in causing image-convergence.

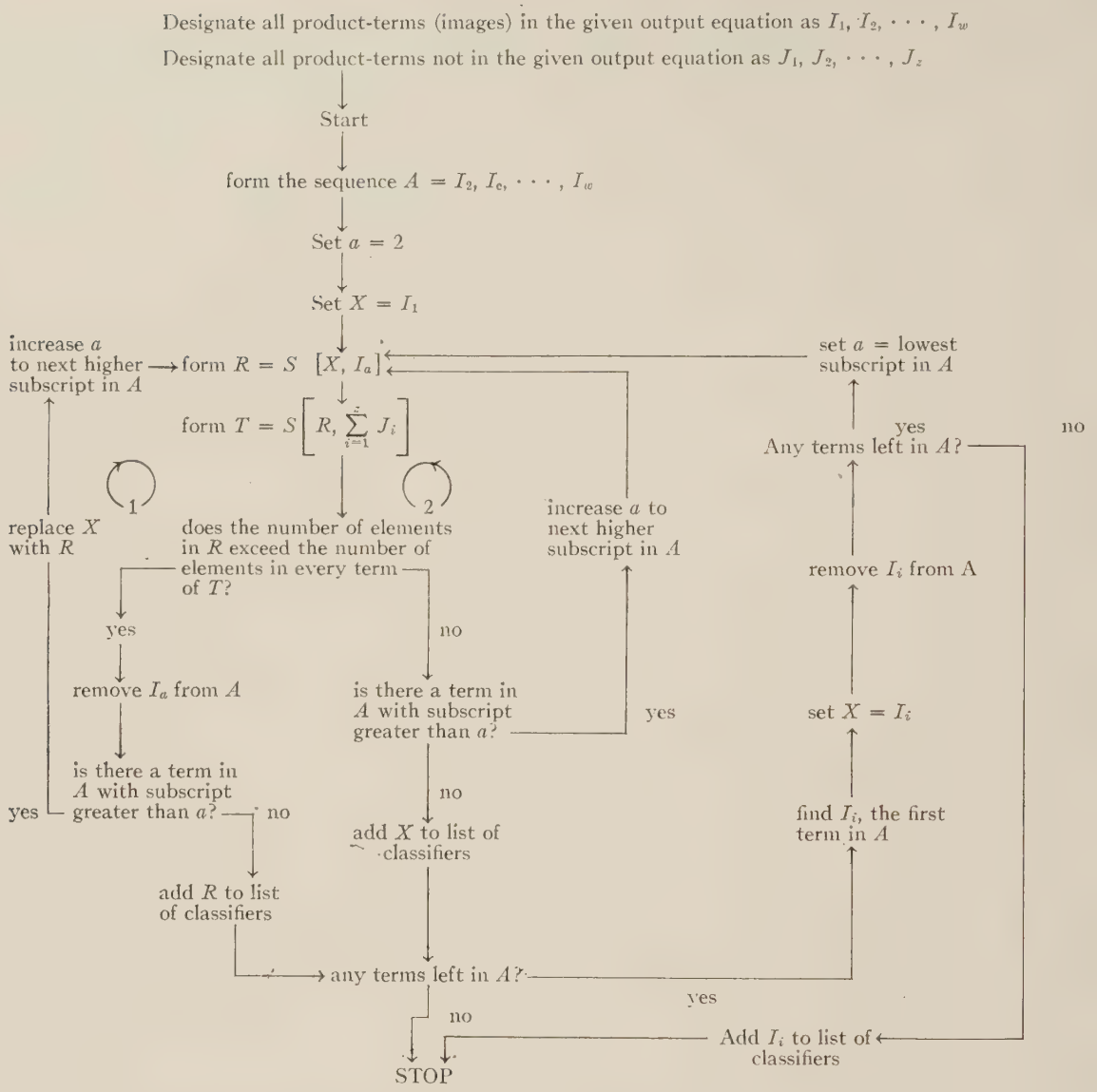


Fig. 6—Flow diagram for computing classifiers for one output.

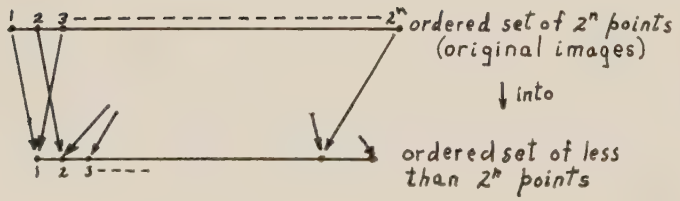


Fig. 7—Convergent mapping of images.

Appendix

Example Following Fig. 6

In the equations in (4), let $n=6$ and let $I_k=2$ for $K=1, 2, \cdots, 8$, so that each of the 8 patterns has two images. All images are shown in Fig. 8. The equation

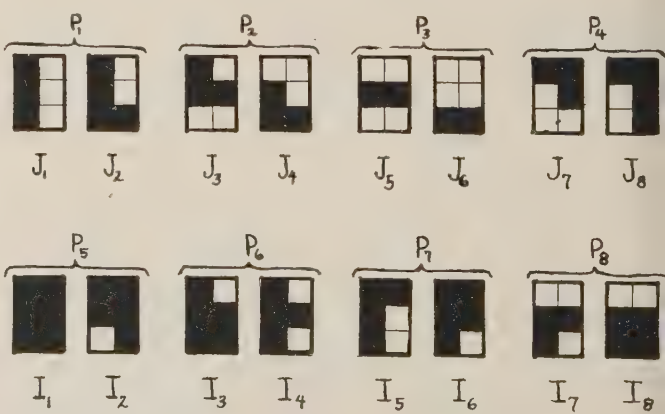


Fig. 8.

r O_1 is to be reduced in this example; hence, the ages in Fig. 8 are labeled I_1, I_2, $\cdots$, I_8 and J_1, , $\cdots$, J_8, to conform with lines 1 and 2 of Fig. 6. hat is,

$$O_1 = \sum_{K=5,6,7,8} \sum_{j=1}^{2} \prod_{i=1}^{6} e_i^{(qijk)} = \sum_{i=1}^{8} I_i. \tag{8}$$

conform with the notation in Fig. 6. For example, te that, with elements numbered as in Fig. 4,

$$I_2 = e_1^1 e_2^1 e_3^1 e_4^1 e_5^0 e_6^1.$$

llowing the flow chart, these steps are now taken:

1) Start.
2) Form sequence $A = I_2, I_3, I_4, I_5, I_6, I_7, I_8$.
3) Set $a = 2$.
4) Set $X = I_1$.
5) Form

$$R = S(X, I_a) = S(I_1, I_2)$$
$$= S(e_1^1 e_2^1 e_3^1 e_4^1 e_5^1 e_6^1,\ e_1^1 e_2^1 e_3^1 e_4^1 e_5^0 e_6^1) = e_1^1 e_2^1 e_3^1 e_4^1 e_6^1.$$

6) Form

$$T = S\left(R, \sum_{i=1}^{8} J_i\right)$$
$$= S[e_1^1 e_2^1 e_3^1 e_4^1 e_6^1,\ (e_1^1 e_2^0 e_3^1 e_4^0 e_5^1 e_6^0 + e_1^1 e_2^0 e_3^1 e_4^0 e_5^1 e_6^1$$
$$+ e_1^1 e_2^0 e_3^1 e_4^1 e_5^0 e_6^0 + e_1^0 e_2^0 e_3^1 e_4^1 e_5^1 e_6^1 + e_1^0 e_2^0 e_3^1 e_4^1 e_5^0 e_6^0$$
$$+ e_1^0 e_2^0 e_3^1 e_4^1 e_5^1 e_6^1 + e_1^1 e_2^0 e_3^1 e_4^1 e_5^1 e_6^1 + e_1^1 e_2^0 e_3^1 e_4^1 e_5^0 e_6^1)]$$
$$= e_1^1 e_3^1 + e_1^1 e_3^1 e_6^1 + e_1^1 e_3^1 e_4^1 + e_3^1 e_6^1 + e_3^1 e_4^1 + e_6^1$$
$$+ e_1^1 e_2^1 e_4^1 + e_1^1 e_2^1 e_4^1 e_6^1.$$

7) Does the number of elements in $(e_1^1 e_2^1 e_3^1 e_4^1 e_6^1)$ exceed the number of elements in every term of T? *Yes.*
8) $A = I_3, I_4, I_5, I_6, I_7, I_8$.
9) Is there a term in A with subscript greater than 2? *Yes.*
10) $X = R = e_1^1 e_2^1 e_3^1 e_4^1 e_6^1$.
11) Increase a to $a = 3$.
12) $R = (e_1^1 e_2^1 e_3^1 e_4^1 e_6^1,\ I_3) = e_1^1 e_3^1 e_4^1 e_6^1$.
13) $T = S\left(R, \sum_{i=1}^{8} J_i\right) = e_1^1 e_3^1 + e_1^1 e_3^1 e_6^1 + e_1^1 e_3^1 e_4^1 + e_3^1 e_6^1$
$+ e_3^1 e_4^1 + e_6^1 + e_1^1 e_4^1 + e_1^1 e_4^1 e_6^1$.
14) [Same as step 7) with $R = e_1^1 e_3^1 e_4^1 e_6^1$.] *Yes.*
15) $A = I_4, I_5, I_6, I_7, I_8$.
16) [Same as step 9) with $a = 3$.] *Yes.*
17) $X = R = e_1^1 e_3^1 e_4^1 e_6^1$.
18) Increase a to $a = 4$.
19) $R = S(e_1^1 e_3^1 e_4^1 e_6^1,\ I_4) = e_1^1 e_3^1 e_4^1$.
20) $T = e_1^1 e_3^1 + e_1^1 e_3^1 + e_1^1 e_3^1 e_4^1 + \cdots$.
21) [Same as step 7) with $R = e_1^1 e_3^1 e_4^1$.] *No*, because of 3rd term in T.
22) [Same as step 9) with $a = 4$.] *Yes.*
23) Increase a to $a = 5$.
[Note that steps 5) through 11) and steps 12) through 18) were passes through loop 1 on Fig. 6, while steps 19) through 23) represented a pass through loop 2.)
24) Pass through loop 2 three more times, so that now $a = 8$ and $A = I_4, I_5, I_6, I_7, I_8$.
25) $R = S(X, I_a) = S(e_1^1 e_3^1 e_4^1 e_6^1,\ e_1^0 e_2^0 e_3^1 e_4^1 e_5^1 e_6^1)$
$= e_3^1 e_4^1 e_6^1$.
26) $T = e_3^1 + e_3^1 e_6^1 + e_3^1 e_4^1 + e_3^1 e_6^1 + e_3^1 e_4^1 + e_6^1 + e_4^1$
$+ e_4^1 e_6^1$.
27) [Same as step 7) with $R = e_3^1 e_4^1 e_6^1$.] *Yes.*
28) $A = I_4, I_5, I_6, I_7$.
29) [Same as step 9) with $a = 8$.] *No.*
30) Add the first classifier, $e_3^1 e_4^1 e_6^1$, to the list of classifiers. Images I_1, I_2, I_3 and I_8 are now "classified."
31) Any terms left in A? *Yes.*
32) $I_1 = I_4$, $X = I_4$, $A = I_5, I_6, I_7$. Any terms left in A? *Yes.*
33) Set $a = 5$.
34) Form $R = e_1^1 e_3^1 e_5^1 e_6^0$ and pass through loop 2. (Note that now $a = 6$.)
35) Form $R = e_1^1 e_3^1 e_4^1 e_5^1 e_6^0$ and pass through loop 1. (Note that now $A = I_5, I_7$.)
36) $R = e_3^1 e_4^1 e_5^1 e_6^0$.
37) $T = e_3^1 e_5^1 e_6^0 + e_3^1 e_5^1 + e_3^1 e_4^1 e_6^0 + \cdots$.
38) [Same as step 7) with $R = e_3^1 e_4^1 e_5^1 e_6^0$.] *Yes.*
39) $A = I_5$.
40) [Same as step 9) with $a = 7$.] *No.*
41) Add second classifier, $e_3^1 e_4^1 e_5^1 e_6^0$, to list of classifiers. (This one classifies I_4, I_6 and I_7.)
42) Any terms left in A? *Yes.*
43) $I_1 = I_5$, $X = I_5$, A is empty. Any terms left in A? *No.*
44) Add $I_5 = e_1^1 e_2^1 e_3^1 e_4^0 e_5^1 e_6^0$ to list of classifiers.
45) Stop.

The list of classifiers is complete, and

$$O_1 = \text{sum of classifiers}$$
$$= e_3^1 e_4^1 e_6^1 + e_3^1 e_4^1 e_5^0 e_6^1 + e_1^1 e_2^1 e_3^1 e_4^0 e_5^1 e_6^0. \tag{9}$$

This is clearly simpler than (8). On the other hand, a *minimal* second-order form for (8) is

$$O_1 = e_4^1 e_5^1 + e_2^1 e_3^1. \tag{10}$$

Thus, the method of classifiers usually reduces output equations like (4), but, in general, it does not minimize them. It is, therefore, useful when the number of variables n is large, and ordinary minimization methods[2] cannot be applied.

Optimization of Reference Signals for Character Recognition Systems*

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Summary—The role of signal structure in a signal discrimination system is discussed. The optimality criterion for reference signals for detection in the case of white Gaussian independent noise is defined. The need for normalization of the reference signals is demonstrated. A geometric interpretation is presented. Optimum classes are obtained and several examples cited. A theoretical optimum class of signals is derived against which any set of signals developed within given constraints may be rated.

Introduction

THIS paper has arisen from a study for applying character recognition to obtain information from documents to be automatically processed. In this connection, it is necessary to find means for placing information on the documents in the form of printed characters which can be identified unambiguously by humans and yet can be read easily by machine means.

An analog method for the detection of such signals is assumed here. The problem is to develop a system which can read humanly identifiable characters with an acceptable degree of certainty and under typical conditions of document mutilation. One task is to find a system of reference signals that is optimum. One criterion for evaluation is the average risk presented by the system. This requires setting costs for correctly identifying a character, for incorrectly identifying a character, and for refusing to identify a character (rejection). A mathematical model is then constructed, and it is possible to derive an optimum system mathematically.

Work has been done in this field by Middleton and Van Meter,[1,2] and by Chow.[3] It has been shown by them that the optimum structure for a detection system depends to a large degree on the type and amount of noise encountered in the recognition process. The optimum system has been derived with a rejection region and practical cost assignments for Gaussian white noise. This solution, though a simplification of the signal recognition problem, serves as a good standard of comparison for evaluating a signal recognition system.

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[1] D. Middleton and D. Van Meter, "Detection and extraction of signals in noise from the point of view of statistical decision theory," *J. Soc. Ind. Appl. Math.*, vol. 3, pp. 192–253, December, 1955; and vol. 4, pp. 86–119, June, 1956.

[2] D. Middleton and D. Van Meter, "On optimum multiple-alternative detection of signals in noise," IRE TRANS. ON INFORMATION THEORY, vol. IT-1, pp. 1–8; September, 1955.

[3] E. K. Chow, "Optimum character recognition system using decision function," 1957 IRE WESCON CONVENTION RECORD, pt. 4, pp. 121–129.

Although the noise encountered is usually band limited, the means of generating the signals imposes a similar limitation, so that the assumption of white noise is not prejudicial. Again, the noise seems to be influenced to some extent by the signal, among other factors, but this effect varies greatly so that it appears to take on a Gaussian property in the large.

Once a system has been decided upon, there is still the problem of character design. Complete freedom in the choice of signal structure has been assumed by Chow and by Middleton and Van Meter. Two signals that differ only slightly come from characters which are very similar in appearance. It is difficult for both the human and the machine to distinguish between such characters, especially with mutilation present. Therefore, the greater the differences among the characters in the character set, the easier it is to distinguish each character.

It is the purpose of this paper to study the structure of the reference signals in order to determine the best set on the basis of complete freedom of choice of the signals. This would provide a standard toward which improvement in signal structure could be directed. The alphabetic characters could not possibly be such as to generate the optimum signals. This is because the requirements of human identifiability place a constraint upon the design of the original characters from which the signal is derived.

No attempt is made to set up rules or methods for making a practical design of a set of characters. The goal is to set a target towards which to strive in designing such a set of characters.

Assumptions

The assumptions to be made in this exposition are: the system of detection to be used is the optimum mathematical system based on a minimum risk decision; the noise present is white Gaussian noise; no reject region is present; the criterion for optimization is that of "Bayes risk" or minimization of average cost as in Middleton and Van Meter;[1,2] and the system is one using correlation functions and analog detection.

The symbols used below are defined in Appendix I.

Sample Signals

To delimit our problem, the waveforms to be dealt with will be considered as sampled. We will consider K character signals; each signal will be sampled at N distinct points. A signal $\tilde{S}_i$ is an amplitude varying function

time, $\tilde{S}_i = \tilde{S}_i(t)$. All signals are assumed to be zero outside the interval $0 \leq t \leq T$. Let us divide this interval to N equal parts, each of length T/N. Let $t_1 = T/N$, $= 2T/N, \cdots, t_N = T$. Then we have created N equidistant sampling times. The amplitude of the signal $\tilde{S}_i$ a given sampling time t_α will be given by the use of wo subscripts: $S_{i\alpha} = S_i(t_\alpha)$. The first signal is indicated elow; the tilde ($\sim$) is used to indicate that it is composed of several vector components; $\tilde{S}$ is to be used for ny signal; the subscript 1 indicates the first signal.

$$\tilde{S}_1 = (S_{11}, S_{12}, \cdots, S_{1N}). \tag{1}$$

ny other signal, say the ith one, would be given as

$$\tilde{S}_i = (S_{i1}, S_{i2}, \cdots, S_{iN}). \tag{2}$$

hese signals can be thought of as vectors in an N-imensional abstract space. The components of each ector correspond to the time sample. Thus, the first mponent, S_{i1} of $\tilde{S}_i$ represents the value of $S_i(t)$ when $= t_1$. The length of a vector drawn from the origin to point in space is the diagonal of an orthogonal paralotope whose edges are the components of the vectors ong the coordinate axes. This length is indicated by ertical lines enclosing the vector and is defined as

$$|\tilde{S}_i| = \sqrt{\sum_\alpha S_{i\alpha}^2}. \tag{3}$$

Let us now set up a model of our multisignal system. he reference signal for each character is represented by vector emanating from the origin. The components of ach vector represent the magnitude of the idealized ample values. An unknown waveform to be identified is epresented by the vector $\tilde{V}$. The unknown vector is not mited in magnitude. It is composed of some multiple f one reference signal, and random noise, $\tilde{V} = c\tilde{S}_i + \tilde{N}$. ts length represents rms power content and its comonents its sample values. The problem presented in his model is to identify the source signal or signal class f the unknown signal vector $\tilde{V}$.

Criteria

The criteria used to peg an unknown signal into a ignal class depend upon the type of noise and intererence present in the system. The various kinds of intererence which are encountered have been discussed elsewhere.[1,3] Random white Gaussian noise is most easily andled analytically. This problem is discussed in other ources.[1,2] The appropriate decision criterion is based on he cross correlation functions between the observed, nd each of the reference, signals. The observed signal $\tilde{V}$ is the sum of two vectors,

$$\tilde{V} = c\tilde{S}_i + \tilde{N} \tag{4}$$

where $\tilde{N}$ is the noise vector whose components are independent random variables, and c is some positive constant corresponding to an amplification or degradation actor.

The cross correlation function to be used as a criterion is

$$\phi_i = \sum_\alpha S_{i\alpha} V_\alpha. \tag{5}$$

This may be expressed in terms of the vectors as

$$\phi_i = \tilde{S}_i \cdot \tilde{V}. \tag{6}$$

The decision as to what signal class (positive multiples of a reference signal) the unknown signal $\tilde{V}$ belongs is made by examining the various ϕ_i and choosing the largest number.

The Need for Normalization of the Reference Signals, S_i

The need for equal-power reference signals is demonstrated graphically in Fig. 1 where there appear three

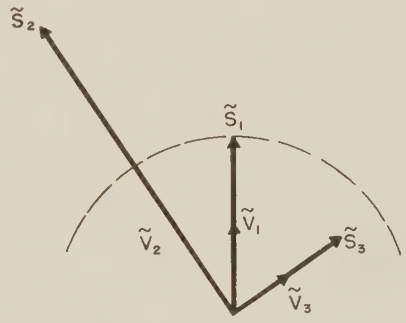

Fig. 1—Illustrating the need to normalize.

signal vectors, $\tilde{S}_1$, $\tilde{S}_2$, and $\tilde{S}_3$. $\tilde{S}_1$ is chosen as a unit vector; the length of $\tilde{S}_2$ is greater than 1; the length of $\tilde{S}_3$ is less than 1. Consider an incoming vector $\tilde{V}_1$ to be identified. Let it be a multiple K_1 of the signal $\tilde{S}_1$. Let us try to use the cross correlation coefficient to determine from whence $\tilde{V}_1$ was obtained. From our assumption, $|\tilde{V}| = K_1$. Then the cross correlation of $\tilde{S}_1$ and $\tilde{V}_1$ is given by

$$\phi(\tilde{S}_1, \tilde{V}_1) = \tilde{S}_1 \cdot \tilde{V}_1 \tag{7}$$

or

$$= (\cos < \tilde{S}_1, \tilde{V}_1) |\tilde{S}_1| \, |\tilde{V}_1| \tag{8}$$

and

$$\phi(\tilde{S}_1, \tilde{V}_1) = 1 \cdot 1 \cdot K_1 = K_1. \tag{9}$$

The cross correlation of S_2 (larger than S_1) is given by

$$\phi(\tilde{S}_2, \tilde{V}_1) = \tilde{S}_2 \cdot \tilde{V}_1 \tag{10}$$

or

$$\phi(\tilde{S}_2, \tilde{V}_1) = (\cos < \tilde{S}_2, \tilde{V}_1) |\tilde{S}_2| \, |\tilde{V}_1| \tag{11}$$

and

$$\phi(\tilde{S}_2, \tilde{V}_1) = \phi_{12} K_1 K_2 \tag{12}$$

where the length of $\tilde{S}_2$ is K_2, and ϕ_{12} is the cross correlation between $\tilde{S}_1$ and $\tilde{S}_2$.

The wrong conclusion would be drawn if the correla-

tion in (7) were smaller than that in (10), *i.e.*, if

$$\phi(\tilde{S}_1\tilde{V}_1) < \phi(\tilde{S}_2\tilde{V}_1) \tag{13}$$

which implies

$$K_1 < \phi_{12}K_1K_2 \tag{14}$$

or

$$1/\phi_{12} < K_2. \tag{15}$$

This result states that if the length of $\tilde{S}_2$ is greater than $1/\phi_{12}$, $\tilde{V}_1$ may be mistaken for $\tilde{S}_2$.

In a similar fashion it may be shown that

$$\phi(\tilde{S}_3, \tilde{V}_3) < \phi(\tilde{S}_1, \tilde{V}_3) \tag{16}$$

if

$$K_1K_3^2 < K_1K_3\phi_{13} \quad \text{or} \quad K_3 < \phi_{13}. \tag{17}$$

Thus, if the signal vectors are not normalized, misidentification may occur.

In what follows, all signal reference vectors are of unit length.

Geometric Interpretation

The correlation coefficient is the scalar product of the unknown and the signal vectors. A two-dimensional model of the system is shown in Fig. 2. Since the reference signals are of unit length, the scalar product is given by

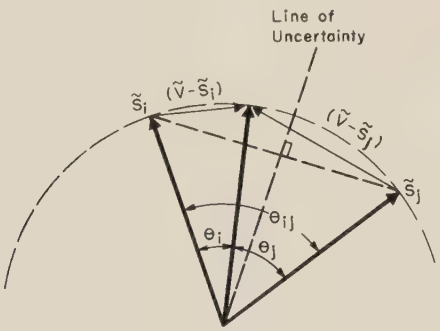

Fig. 2—Geometry for identifying unknown vector V.

$$\phi_i = S_i\tilde{V} = k\cos\theta_i \tag{18}$$

where k is the length of V and θ_i the angle between $\tilde{V}$ and $\tilde{S}_i$. Thus, in comparing $\tilde{V}$ with all the reference signals, the comparison is among the $k\cos\theta_i$. Since the k is common to each of these terms, this is actually a comparison of $\cos\theta_i$ for a maximum. This in turn is a comparison of the θ_i. We inspect the angles made by $\tilde{V}$ with each of the reference signals $\tilde{S}_i$ in turn and look for the reference signal with which $\tilde{V}$ makes the smallest angle. It is safest to identify this reference signal as the source of $\tilde{V}$.

This criterion is the same as finding the closest signal vector to $\tilde{V}$. The distance between the terminal points of $\tilde{S}_i$ and $\tilde{V}$, or simply, the distance between the two vectors, is defined as

$$|\tilde{V} - \tilde{S}_i|^2 = \sum_\alpha (V_\alpha - S_{i\alpha})^2$$

$$= \sum_\alpha (V_\alpha^2 - 2V_\alpha S_{i\alpha} + S_{i\alpha}^2) \tag{19}$$

$$= |\tilde{V}|^2 - 2\tilde{V}\cdot\tilde{S}_i + |\tilde{S}_i|^2. \tag{20}$$

Now

$$|S_2| = 1, \qquad |\tilde{V}| = k, \qquad \tilde{V}\cdot\tilde{S}_i = k\cos\theta_i. \tag{21}$$

Therefore,

$$|\tilde{V} - \tilde{S}_i|^2 = 1 + k^2 - 2k\cos\theta_i. \tag{22}$$

If $\tilde{V}$ is closer to $\tilde{S}_i$ than to $\tilde{S}_j$, then

$$|\tilde{V} - \tilde{S}_i| < |\tilde{V} - \tilde{S}_j| \tag{23}$$

or

$$|\tilde{V} - \tilde{S}_i|^2 < |\tilde{V} - \tilde{S}_j|^2 \tag{24}$$

and

$$1 + k^2 - 2k\cos\theta_i < 1 + k^2 - 2k\cos\theta_j \tag{25}$$

or

$$\cos\theta_j < \cos\theta_i \tag{26}$$

which is the same as

$$\theta_i < \theta_j. \tag{27}$$

Our criterion for classifying $\tilde{V}$ may be stated as follows: $\tilde{V}$ is identified as $\tilde{S}_i$ if the angle it makes with that vector is smaller than that which it makes with any other reference signal, or alternatively, if the distance between the terminal points of $\tilde{V}$ and $\tilde{S}_i$ is less than the distance between the terminal points of $\tilde{V}$ and any other vector.

Optimum Systems

Now let us examine systems of signal vectors. What relationship among the signals in the system will enable us to determine best to what signal class an incoming signal, $\tilde{V}$, belongs?

In Fig. 3 there are two reference signals of unit length, $\tilde{S}_i$ and $\tilde{S}_j$, θ_{ij} is the angle between them, and OB is the

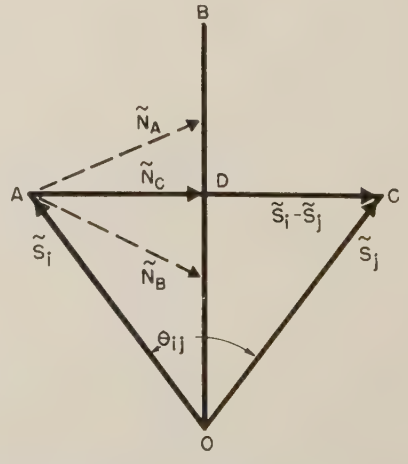

Fig. 3—Determinatoin of minimum tolerable noise N_C.

gle bisector. Any vector from O in the plane and lying thin the angle AOB is identified as $\tilde{S}_i$; any vector lying the angle BOC is identified as $\tilde{S}_j$.

What is the least amount of noise which will corrupt to make it unidentifiable (on OB) or misidentified ithin BOC)? The point on OB which is nearest to A D, which is on the perpendicular to OB through A. ote that line ADC is defined by the vector $\tilde{S}_i - \tilde{S}_j$. The ast noise which would corrupt $\tilde{S}_i$ (to look like $\tilde{S}_j$) is $\tilde{N}_c|$ or sin $(\theta_{ij}/2)$.

This comment still holds when the geometry is exnded to N dimensions. The bisector of angle AOC is en a hyperplane through OB, but $|\tilde{N}_c|$ is still the ast noise which corrupts $\tilde{S}_i$ (to look like $\tilde{S}_j$).

If we are free to move the vectors within system reictions, it is found that the greater the distance beeen the two signal vectors, the more noise is tolerable. creasing the angle between the two signal vectors acmplishes the same thing and similarly improves the stem since $|\tilde{N}_c| = \sin(\theta_{ij}/2)$.

The weakest aspect of any system is reflected by the hallest vector angle of the system. To improve such a stem, this smallest angle must be improved; to find e optimum system, it is necessary to find the *maxium* solution for the *minimum* of the angles formed by ıy two vectors. This, of course, may be restated in rms of the distance between vector terminal points—e minimum distance between pairs of vector terminal oints must be maximized.

The above condition may be restated as maximizing ie minimum cross correlation between any two signal ectors. This may be shown to be true analytically, as llows. Let us examine the incoming signal $\tilde{V}$ which is ie sum of the signal $\tilde{S}_i$ and noise, $\tilde{N}$. The correlation $\tilde{V}$ with $\tilde{S}_i$ and $\tilde{V}$ with $\tilde{S}_j$ is given in (28) and (29), and 30) and (31).

$$\phi_i = \tilde{V}\cdot\tilde{S}_i = (\tilde{S}_i + \tilde{N})\cdot S_i \tag{28}$$

$$= \tilde{S}_i\cdot\tilde{S}_i + \tilde{N}\cdot\tilde{S}_i = 1 + \tilde{N}\cdot\tilde{S}_i \tag{29}$$

$$\phi_j = \tilde{V}\cdot\tilde{S}_j = (\tilde{S}_i + \tilde{N})\cdot S_j \tag{30}$$

$$= \tilde{S}_i\cdot\tilde{S}_j + \tilde{N}\cdot\tilde{S}_j = \phi_{ij} + \tilde{N}\cdot\tilde{S}_j \tag{31}$$

here ϕ_{ij} is the correlation between $\tilde{S}_i$ and $\tilde{S}_j$. Disnguishability will be lowest when the results of (29) nd (31) are equal. The equality leads to these equaons:

$$1 + \tilde{N}\cdot\tilde{S}_i = \phi_{ij} + \tilde{N}\cdot\tilde{S}_j \tag{32}$$

$$\tilde{N}\cdot(\tilde{S}_j - \tilde{S}_i) = 1 - \phi_{ij}. \tag{33}$$

Now

$$\tilde{N}\cdot(\tilde{S}_j - \tilde{S}_i) = |\tilde{N}|\,|\tilde{S}_j - \tilde{S}_i|\cos\psi \tag{34}$$

here ψ is the angle between $\tilde{N}$ and $(\tilde{S}_j - \tilde{S}_i)$. We are nterested in the least corrupting noise, $|N_c|$ for $\tilde{N}$ for hich (32) holds true. Then from (33) and (34),

$$|\tilde{N}|\,|\tilde{S}_j - \tilde{S}_i|\cos\psi = 1 - \phi_{ij} \tag{35}$$

or

$$|\tilde{N}| = \frac{1 - \phi_{ij}}{|\tilde{S}_j - \tilde{S}_i|\cos\psi}. \tag{36}$$

Obviously $|\tilde{N}|$ is a minimum for $\cos\psi = 1$. Then (35) becomes

$$|N_c|\,|\tilde{S}_j - S_i| = 1 - \phi_{ij}. \tag{37}$$

Squaring both sides,

$$\tilde{N}_c^2(\tilde{S}_j^2 + \tilde{S}_i^2 - 2S_iS_j) = (1 - \phi_{ij})^2. \tag{38}$$

Since $\tilde{S}_i$ and $\tilde{S}_j$ are unit vectors,

$$\tilde{N}_c^2(1 + 1 - 2\phi_{ij}) = (1 - \phi_{ij})^2 \tag{39}$$

$$2\tilde{N}_c^2 = 1 - \phi_{ij} \tag{40}$$

$$|\tilde{N}_c| = \sqrt{\frac{1 - \phi_{ij}}{2}}. \tag{41}$$

Eq. (41) states that the minimum tolerable corrupting noise increases as the cross correlation becomes smaller. The minimum corrupting noise for the system of signals thus depends upon the smallest angle which exists between *any* two vectors in the system. Then maximizing the smallest angle between any two vectors in the system of reference signals constitutes an optimization of the system.

Mathematical Optimization

We are thus led to the following extremum problem: given K points $X_1, X_2, \cdots, X_K$ on the N-dimensional unit sphere, what is the largest angle α such that the angular distance between any pair of points is at least α? Phrased another way, we wish to find the largest α satisfying

$$X_i\cdot X_j \leq \cos\alpha \qquad i,j = 1, 2, \cdots, K \quad i \neq j. \tag{42}$$

It is clear that α is a function of K and N, say $\alpha(K, N)$. Interestingly enough, there are a number of physical applications which have led to this problem[4] so that the complete solution is of considerable interest. In what follows we prove or give references to proofs of the results obtained up to the present time. We begin by considering two results of a general nature.

Theorem 1:

For $N \geq K-1$, $\alpha(K, N) = \cos^{-1}(-1/K-1)$.

Proof:

We prove first that $\alpha(K, N) \leq \cos^{-1}(-1/K-1)$ for all N and then by construction that the equality sign holds when $N \geq K-1$.

[4] L. L. Whythe, "Unique arrangements of points on a sphere," *Amer. Math Monthly*, vol. 59, pp. 606–611; 1952.

Let K points satisfying (1) be given by $X_1, X_2, \cdots, X_K$ where

$$X_i = (x_{i1}, x_{i2}, \cdots, x_{iN}) \qquad i = 1, 2, 3, \cdots, K$$

with

$$\sum_{j=1}^{N} x_{ij}^2 = 1$$

and consider the function

$$I(X_1, X_2, \cdots, X_K) = (x_{11} + \cdots + x_{K1})^2 + \cdots + (x_{1N} + \cdots + x_{KN})^2. \qquad (43)$$

Expanding, we obtain

$$I(X_1, X_2, \cdots, X_K) = K + 2 \sum_{i} \sum_{\substack{j \\ i<j}} X_i \cdot X_j \qquad i, j = 1, 2, \cdots, K. \qquad (44)$$

Since $I(X_1, X_2, \cdots, X_K) \geq O$ being a sum of real squares

$$K + 2 \sum_{i} \sum_{\substack{j \\ i<j}} X_i \cdot X_j \geq O \qquad i, j = 1, 2, \cdots, K. \qquad (45)$$

By assumption $X_i \cdot X_j \leq \cos \alpha$, hence

$$K + K(K-1) \cos \alpha \geq O \qquad (46)$$

$$\cos \alpha \geq \frac{-1}{K-1} \qquad (47)$$

which proves that for all N

$$\alpha(K, N) \leq \cos^{-1}\left(\frac{-1}{K-1}\right).$$

We shall show that for $N \geq K-1$ one can construct a set of points giving equality in inequality (47). These points are in fact the vertices of the regular $K-1$ dimensional simplex inscribed in the N-dimensional unit sphere. The proof is due to Rankin.[5] We suppose that the N-dimensional unit sphere S_N is the intersection of S_{N+1} with the hyperplane $X_1 + X_2 + \cdots + X_{N+1} = 0$. For X_v, $1 \leq v \leq K$ we let

$$x_{vj} = -\frac{\lambda}{K} \qquad j \neq v, j \leq K$$

$$x_{vv} = \lambda - \frac{\lambda}{K}$$

$$x_{vj} = 0 \qquad j > K \qquad (48)$$

where

$$\lambda = \sqrt{\frac{K}{K-1}}.$$

[5] R. A. Rankin, "The closest packing of spherical caps in N dimensions," *Proc. Glasgow Math. Assoc.*, vol. 2, p. 139; 1955.

The length of X_v is given by

$$\sqrt{\frac{(K-1)\lambda^2}{K^2} + \left(\lambda - \frac{\lambda}{K}\right)^2} = 1.$$

While

$$\sum_{j=1}^{K} x_{vj} = \frac{-(K-1)\lambda}{K} + \lambda - \frac{\lambda}{K} = 0$$

and

$$X_v \cdot X_t = \frac{(K-2)\lambda^2}{K^2} - 2\left(\lambda - \frac{\lambda}{K}\right)\frac{\lambda}{K} = \frac{-1}{K-1}$$

$$v \neq t$$

$$v, t = 1, 2, \cdots, K.$$

From this the theorem follows.

Theorem 2:

For $N+2 \leq K \leq 2N$, $\alpha(K, N) = \pi/2$.

This result was first proved by Hajos and Davenport; however, an elegant proof due to Rankin[5] exists. It is easily seen that $\alpha(K, N) \geq \pi/2$ since one can always select the points from the set $(\pm 100 \cdots 0) \cdots (000 \cdots \pm 1)$.

In view of Theorems 1 and 2, it is sufficient for a given N to look only at the cases $K \geq 2N+1$. We now examine particular spaces.

Case I. $N=2$

The solution is trivial and is easily seen to be

$$\alpha(K, 2) = \frac{2\pi}{K}. \qquad (49)$$

Case II. $N=3$

Exact solutions are known for $K=7$, 8, 9, and 12. The first three cases were proved in 1951 by Van Der Waerden and Schütte,[7] which is an indication of the difficulty of the problem. Their findings are summarized in Table I.[8]

For $K=10$, 11, 13, 14, 15, 16, 24, and 32, Van Der Waerden and Schütte were able to construct a set of points such that the minimum distance between any pair is given by the smaller entry in the table. The larger entry depends on a result due to L. Féjes Toth[9] which gives an asymptotic upper bound for $\alpha(K, 3)$.

$$\alpha(K, 3) \leq \cos^{-1}\left[\frac{1}{2}\left(\cot^2 \frac{K\pi}{6(K-2)} - 1\right)\right] = \alpha^*(K, 3). \qquad (49a)$$

[6] H. Davenport and G. Hajos, "Aufgabe 35," *Matematikai Lapok*, vol. 2, p. 68; 1951.

[7] K. Schütte and B. L. Van Der Waerden, "Auf Welcher Kugel Haben 5, 6, 7, 8, oder 9 Punkte mit Mindestabstand 1 Platz?," *Math. Ann.*, vol. 123, p. 195, and vol. 124, p. 96.

[8] L. Féjes Toth, "Lagerungen in der Ebenen auf der Kugel und im Raum," Springer-Verlag, Berlin, Ger.; 1953.

[9] L. Féjes Toth, "On the densest packing of spherical caps," *Amer. Math. Monthly*, vol. 56, pp. 330–331; 1949.

TABLE I

MAXIMUM VALUE OF MINIMUM ANGLE FOR K VECTORS IN THREE DIMENSIONS, $\alpha(K, 3)$

K	$\alpha(K, 3)$
7	$\cos^{-1}(\cot 80° - \cot 40°)$
8	$\cos^{-1}[(\sqrt{8}-1)/7]$
9	$\cos^{-1}(1/3)$
10	66°19′ — 69°33′42″
11	63°26′06″ — 66°17′23″
12	63°26′06″
13	57°08′ — 60°55′11″
14	55°40′ — 58°40′51″
15	53°39′ — 56°40′01″
16	52°14′ — 54°51′19″
24	43°41′ — 44°42′52″
32	37°22′ — 38°41′31″

This bound is exact for $K=3$, 4, 6 and 12. Table II ves Toth's bound for $K \leq 50$ to the nearest hundredth a degree.

ase III. $N=4$, $K \geq 9$

The only exact solution that is known occurs for =120, $\alpha(120, 4) = 36°$. The points are the vertices of a gular polygon in 4-space with 120 vertices.

For $N \geq 5$ and $K \geq 2N+1$ no solutions are apparently iown. Outside of the solutions we have described, the est that is presently available are some upper bounds ıe to R. A. Rankin.[10] Rankin considers the inverse roblem: Given an angle 2α on the N-dimensional unit here, what is the maximum number of points K such iat any pair have an angular distance of at least 2α? etting $K = M(\alpha, N)$, Rankin obtains the result

$$M(\alpha, N) \leq \frac{\pi^{1/2}\Gamma\left(\frac{N-1}{2}\right)\sin\beta\tan\beta}{2\Gamma\left(\frac{N}{2}\right)\int_0^\beta (\sin\theta)^{N-2}(\cos\theta - \cos\beta)d\theta}$$

$$= M^*(\alpha, N). \tag{50}$$

$$0 < \alpha < \frac{\pi}{4}$$

$$\beta = \sin^{-1}(\sqrt{2}\sin\alpha).$$

or

$$\beta < \cos^{-1}\left(\frac{1}{\sqrt{N}}\right) - e(N), \quad \text{where } e(N) > 0 \text{ and}$$

$$\lim_{N\to\infty} e(N) = 0,$$

$M^*(\alpha, N)$ is a continuous monotonic decreasing function f α for fixed N, and hence, by an elementary theorem f calculus, it has an inverse function $\alpha(K, N)$ which is

[10] R. A. Rankin, "On the minimal points of positive definite iadratic forms," *Mathematika*, vol. 3. pp. 15–24; 1956.

TABLE II

ASYMPTOTIC MAXIMUM VALUE OF MINIMUM ANGLE FOR K VECTORS IN THREE DIMENSIONS, $\alpha^*(K, 3)$, TO NEAREST HUNDREDTH OF A DEGREE

K	$\alpha^*(K, 3)$	K	$\alpha^*(K, 3)$
3	120.00	27	42.14
4	109.47	28	41.37
5	98.51	29	40.65
6	90.00	30	39.96
7	83.30	31	39.30
8	77.87	32	38.69
9	73.37	33	38.09
10	69.56	34	37.53
11	66.29	35	36.99
12	63.43	36	36.46
13	60.92	37	35.96
14	58.68	38	35.48
15	56.67	39	35.03
16	54.85	40	34.58
17	53.20	41	34.15
18	51.68	42	33.74
19	50.30	43	33.35
20	49.01	44	32.96
21	47.82	45	32.60
22	46.72	46	32.23
23	45.68	47	31.89
24	44.71	48	31.56
25	43.80	49	31.23
26	42.95	50	30.92

also continuous and monotonic. For computational purposes one can always use (50) as an implicit function to tabulate $M(\alpha, N)$. For $\cos^2 2\alpha < 1/N$, $M^*(\alpha, N)$ fails to give good results. From some work[10] relating to the minimal points of positive definite quadratic forms, Rankin was able to show that if the points are packed in pairs at opposite ends of a diameter, then for $\cos^2 2\alpha < 1/N$

$$K \leq \frac{2N\sin^2 2\alpha}{1 - N\cos^2 2\alpha}. \tag{51}$$

In 1957, Blóh[11] succeeded in improving Rankin's bound,[10] (50), by a factor

$$\left[1 + \left(1 + \frac{\tan^2\beta}{N+1}\right)^{1/2}\right]^{-1}$$

which is only a very slight improvement and this is where the matter rests.

Table III summarizes optimum signal structures for different numbers of signals (K) and different numbers of sample points (N). For combinations of K and N the cosine of the maximum value for the minimum angle between any two signals is given. A proposed system of signals can be compared with this optimum by the maximum correlation coefficient between any two signals in the system.

[11] E. L. Blóh, "On the most dense arrangements of spherical segments on a hypersphere," *Izv. Akad. Nauk. SSSR*, Ser. Mat., vol. 20, pp. 707–712; 1956. (Russian.)

TABLE III

MINIMUM ATTAINABLE CROSS CORRELATION COEFFICIENTS, cos θ

Number N of sample points	Number of signals, K												
	2	3	4	5	6	7	8	9	10	11	12	13	14
2	−1.0	−0.5	0	0.31	0.50	0.62	0.71	cos (360/K) →					
3			−0.33	0	0	0.21	0.26	0.33	0.41	0.44	0.45	0.55	0.57
4				−0.25	0	0	0	—	0.25	—	—	—	—
5					−0.20	0	0	0	0	—	0.20	—	—
6						−0.17	0	0	0	0	0	—	0.17
7							−0.14	0	0	0	0	0	0
8								−0.13	0	0	0	0	0
9									−0.11	0	0	0	0
10										−0.10	0	0	0
11											−0.09	0	0
12												−0.09	0
13													−0.08
Unconditional optimum	−1.0	−0.5	−0.33	−0.25	−0.20	−0.17	−0.14	−0.13	−0.11	−0.10	−0.09	−0.09	−0.08

NOTE: Underscore indicates lower bound; exact value unknown. The bound is obtained by taking the $N+1$ vertices of the regular N-dimer sional simplex and rotating them through an angle of 180°. The resulting $2N+2$ points constitute a set such that any pair satisfies the ir equality

$$X_i \cdot X_j \leq \cos^{-1}\left(\frac{1}{N}\right).$$

CONCLUSIONS

From Theorem I an interesting conclusion can be drawn. This equation states that for a fixed number of vectors, K, if we increase the number of dimensions above $K-1$, the optimum angle will not change. This means that we can find the optimum not only for a given dimension but for any dimension. This is a powerful tool, for it means that, knowing the number of signals with which we must deal, if the number of samples is increased beyond this optimum, the solution will not improve. This might lead us right into a fallacy. The statement above is undeniably true when no restrictions exist as to the construction of the signals. If we now introduce the restrictions imposed by assuming the signals were generated when characters printed in magnetic ink pass under a magnetic reading head, we find that it is impossible to achieve this optimum. If we now increase the number of sample points, we also increase the degrees of freedom for the choice of signal vectors which comprise an optimum or near optimum system. It is then more easily possible to comply with the constraints imposed by the geometry of the characters and still construct a near optimum system. As an example, the polarity and minimum magnitude of certain sample points may be derived from the required geometry as initial constraints imposed upon the system. With the addition of a few sample points, a near optimum solution might be constructed.

The solution for K vectors in $K-1$ dimensions, the solution which, with no constraint imposed, cannot be improved upon, will hereafter be referred to as the unconditional optimum.

A conditionally optimum system (one which could be improved upon by going to more dimensions or sample points) exists when there are twice as many vectors as dimensions. The optimum angle in that case is always 90° and this is an orthogonal system. As the number c signals increases, the unconditionally optimum syster solution gets closer and closer to 90° (see Theorem 1) For ten signals the unconditionally optimum solutio is 96°. The difference between conditional optimum an unconditional optimum is only six degrees.

The case where there are N dimensions or sampl points and the number of signals K is equal to 2^N i almost always far short of the unconditionally optimun system. This problem corresponds to the case of binary coding. Our solution states that if we have a give number of signals and our method of detecting thes signals is a correlation or analog method, the best possi ble means of encoding information would not be binary coding; it would be a method which used a number o sample points at least equal to one less than the numbe of signals.

It is interesting to see how the amount of freedom in creases as the dimension is increased beyond the un conditionally optimum situation. Let us consider thre signals or vectors only. The unconditionally optimun solution for this system is one where the three vectors li in the same plane and make an angle of 120° with each other. The freedom of choice that exists in this solutio is one degree of rotation. The plane containing the thre vectors may be rotated about the origin.

Consider what happens if the vectors can occupy thre dimensions. The three vectors must still lie in the sam plane but now not only can they rotate within tha plane, but the plane itself may rotate to any positio about the origin. Since the position of a plane in spheri cal coordinates is determined by two direction cosine and since the vectors can still rotate within the plane it is seen that three dimensions allows us three degree of freedom, as compared with one degree of freedom i two dimensions.

Appendix I

List of Symbols Used

K Number of signals to be identified.

$\tilde{S}_i = S_i(t)$ The ith reference signal, a time varying function.

T Maximum duration of a reference signal; $S_i(t)$ is zero outside of the interval $0 \leq t \leq T$ for all i.

N The number of sample points used over the interval $0 \leq t \leq T$ to sample the waveforms $S_i(t)$.

t_α The time at which the α sample is taken;

$$t_\alpha = \frac{\alpha T}{n}; \qquad t_\alpha - t_{\alpha-1} = T/n \text{ for all } j.$$

$S_{i\alpha}$ The αth sample of the ith reference waveform $s_i = s_i(t_\alpha)$.

$|\tilde{S}_i|$ The length of the N-dimensional vector, S_i.

$\tilde{S}_i$ The set of all n samples of the reference waveform S_i; a vector; the set $S_i = (s_{i1}, s_{i2}, \cdots, s_{iN})$.

$\tilde{V}$ An unknown signal defined over the interval 0 to T and to be identified to be or not to be one of the reference signals, S_i.

V_α The unknown signal, V, sampled at the time $t = t_\alpha$; $V_\alpha = \tilde{V}(t_\alpha)$.

$\tilde{V}$ The set (vector) of sample points of the signal, V; $\tilde{V} = (v_1, v_2, \cdots, v_n)$.

$$\tilde{V} = (v_1, v_2, \cdots, v_n).$$

$\tilde{N}$ The noise vector, each of whose components n_j is a random variable; n_j has a normal probability distribution.

ϕ_i The correlation coefficient of the two vectors, $\tilde{S}_i$ and $\tilde{V}$ defined using the discrete sample points;

$$\phi_i = \sum_{\alpha=1}^{N} V_\alpha S_{i\alpha}.$$

ϕ_{ij} The correlation between the two signals $\tilde{S}_i$ and $\tilde{S}_j$;

$$\phi_{ij} = \tilde{S}_i \cdot \tilde{S}_j.$$

k The length of V; $k = |V| = \sqrt{\sum V_j^2}$.

K_1, K_2, K_3 Constants.

θ_i The angle between the two vectors V and S_i.

p The probability of occurrence of the signal vector S_i.

q The probability of the absence of a signal.

$F(\tilde{V}/\tilde{S}_i)$ The conditional probability density distribution of V given S_i.

$F(\tilde{V})$ The probability density of noise done.

Λ_i The likelihood ratio for the ith signal, S_i.

γ_i The criterion for choosing the ith signal as the source of V in preference to any other signal, S_j.

Appendix II

The case of the Multiple Alternative Decision Problem is discussed by Middleton and Van Meter.[1,2] The problem of the signals $\tilde{S}_i$ contaminated by white Gaussian noise is discussed there. Certain simplifying assumptions will be made here to apply the results to a practical signal system: 1) the signals occur with equal probability—this will almost be true when dealing solely with numerals and auxiliary signals; 2) the cost of correctly identifying a character is zero; 3) the cost of misidentifying a character is constant—it makes no difference whether we call a "3" a "5" or a "1"; and 4) no rejection region is considered. The likelihood ratios using our symbols are

$$\Lambda_i = \frac{pF(\tilde{V}/\tilde{S}_i^2)}{qF(\tilde{V})} \tag{52}$$

where $F(\tilde{V}/\tilde{S}_i)$ is the conditional probability distribution of $\tilde{V}$ originating from $\tilde{S}_i$ and $F(\tilde{V})$ is the noise distribution. If the noise is independent and of constant variance and mean zero, then

$$F(\tilde{V}) = K \exp\left(-\sum V_\alpha^2/2\sigma^2\right) \tag{53}$$

and

$$F(\tilde{V}/\tilde{S}_i) = K \exp\left(-\sum_\alpha \frac{(V_\alpha - S_{i\alpha})^2}{2\sigma^2}\right) \tag{54}$$

where

$$K = \left[(\pi)^{n/2}\sigma^n\right]^{-1} \tag{55}$$

so that

$$\log \Lambda_i = \frac{\sum (V_\alpha - S_{i\alpha})^2 + \sum V_\alpha^2}{2\sigma^2} + C$$

$$C = \log (p/q) \tag{56}$$

and, after expansion

$$\log \Lambda_i - C = \frac{2\sum V_\alpha S_{i\alpha} - \sum S_{i\alpha}^2}{2\sigma^2}. \tag{57}$$

Now with the assumption of unit power for the reference waveforms, this becomes

$$\frac{\log \Lambda_i - C}{\sigma^2} + \frac{1}{2} = \sum_\alpha V_\alpha S_{i\alpha}. \tag{58}$$

The criterion for choice of S_i as the source of V, designated as γ_i, is based on

$$\gamma_i: 2\Lambda_i < \Lambda_j \quad \text{all} \quad j \neq i. \tag{59}$$

From (59) it follows that

$$\gamma_i: 2\,\frac{\log \Lambda_i - C}{\sigma^2} + \frac{1}{2} > \frac{\log \Lambda_j - C}{\sigma^2} + \frac{1}{2}, \tag{60}$$

which leads to

$$\gamma_i: 2\sum V_\alpha S_{i\alpha} > \sum V_\alpha S_{j\alpha} \quad \text{all} \quad j \neq i, \tag{61}$$

which, of course, is the correlation criterion.

Frequency-to-Period-to-Analog Computer for Flowrate Measurement*

TED W. BERWIN†

Summary—**The Frequency-to-Period-to-Analog Computer is a special purpose nonlinear analog computer which accepts an ac voltage of varying frequency, acts upon the period of each cycle, computes the inverse of the time period, $e=1/T$, and holds the information for the period of the next cycle. Thus, the output voltage is a level which is proportional to the input frequency $f=1/T$ computed once for every cycle. The system is accurate to better than ± 0.5 per cent of 2/3 full scale. Application of the computer is described and results presented for fast readout and recording of gas and liquid turbine type flowmeters. Extensions of the circuits used can produce voltages proportional to ln t or $1/t^2$, for time t greater than a small positive number.**

Introduction

ON-LINE computers for special applications are used in many fields, for example, record equalization in phonographs, tape recorder equalization, first-order equalization for thermocouples [1], second-order compensation for second-order systems such as pressure transducers [2], etc. Although most applications involve linear analog computation, there are some applications where nonlinear computing is desired. This paper describes a special type of nonlinear computer which is directly applicable to accurate measurement of volume flowrate, although it need not be restricted to this application.

The type of flowmeter with which we shall concern ourselves is a turbine type, which consists of a several-bladed turbine in a gas or liquid flowstream. The property of the flowmeter is that the angular velocity of the rotor is proportional to the volume flowrate of fluid through it. Fig. 1 shows an advanced type turbine flowmeter. Note the tandem blades—one turbine is mounte on ball bearings on the shaft of another turbine to redu the effect of bearing friction. In a flowstream both blad rotate at approximately the same speed, and, as a resul the slave turbine bearing friction is reduced to a min mum. A light beam is interrupted by the blades, provi ing frequency information for recording. This metho of measuring flow is the most widely used and the mo accurate. Other methods of providing electrical co version without drag on the rotor are with capacitan or inductance transducers.

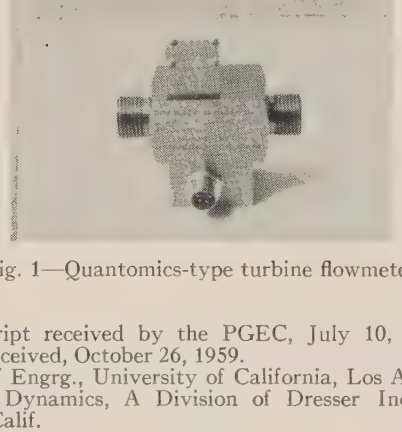

Fig. 1—Quantomics-type turbine flowmeter.

It is of utmost importance to convert and record th electrical information from the flowmeter so that it ca be accurately read out at leisure. Since the output of th flowmeter is an ac voltage whose frequency is propo tional to the flowrate, let us examine methods of inte preting this signal. One obvious method of readout counting the number of cycles for one second and the recording the output digitally. A method commonl used in liquid propellant rocket engine testing is to r cord the voltage waveshape on an oscillograph and the in data reduction to count the number of cycles in a indicated time interval. Another method in frequent us is to convert the frequency into pulses of constant ampl tude and width and then convert these pulses to an ave age value. The output of such a system is a curren proportional to the frequency. The common method c recording this information is on a self-balancing potent ometer since the average voltage amplitudes are in th millivolt range. This method of measurement is ver accurate (± 0.1 per cent) in steady-state, but is ver inaccurate for transients.

The main disadvantage of these methods is that a average count is taken over a relatively long time inte val. Inspection of the information contained in periodic waveshape suggests that the fastest rate a which frequency information may be obtained is onc per cycle. Note that the frequency is given by $f=1/T$ where T is the period of one cycle. It is a relativel simple matter to obtain a digital number proportiona to the period. This has been achieved [3] by opening a electronic gate for a time T and passing clock pulse into a counter (see Appendix I). The output of th counter may be printed on paper, photographed, or rea out as a coded waveshape. This method provides ver accurate (± 1 count in the fourth decimal place) an reliable information at a relatively fast rate (approx mately 20 per second maximum). However, if informa tion of flowrate variation is to be obtained, tediou plotting of hundreds of individual points is necessary

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ie information is also proportional to the inverse of quency, which is rather confusing.

The Frequency-to-Period-to-Analog Computer, here- er to be referred to as FPAC, which is the subject of s paper, is an instrument which operates on the riod T of one cycle of an alternating wave, computes e inverse $1/T$, which is equal to frequency f, and pro- les an analog voltage which is proportional to the erage frequency for each particular cycle. The ad- ntages of such a system are optimum response, high- nsient and steady-state accuracy, and convenient esentation of flowrate data.

Basic System

The Frequency-to-Period-to-Analog Computer ac- pts a periodic voltage of frequency f and provides an itput voltage level proportional to f computed from e period T of each cycle of the input. The basic system in four parts as shown in Fig. 2.

Fig. 2—Basic system.

The Amplifier and Squaring Circuit amplifies and nits the input level so that a constant amplitude uare wave signal of period T is generated. The second ock represents the k/t Computer where k is a con- ant, and t is the variable time. This is the heart of the stem and will be covered in detail. The Sample and old Circuit receives information of voltage level once r every cycle of input and holds it for the length of the ext cycle. The Output Amplifier supplies appropriate ower to drive any type of recording system, for exam- e, a galvanometer in an oscillograph recorder, an os- lloscope, etc.

ealization of $e=k/t$

The heart of the FPAC system is a generator whose itput voltage is $e=k/t$. Inspection of the function ows a discontinuity at $t=0$. Since e approaches in- ity as t approaches zero, the function is not physically alizable at $t=0$; and furthermore, as $T\to 0$, $f\to\infty$, hich is also nonrealizable. Therefore, let us place an per limit on e, thus restricting the upper range to $_{max}$.

In Fig. 3, let

$$e = \begin{cases} E_{max}, & 0 \le t < \alpha \\ E_0\beta/t, & t \ge \alpha. \end{cases} \tag{1}$$

We shall consider the function only for $t\geq 0$ in this scussion.

The problem now becomes one of generating a voltage escribed by (1). Assuming that there are several ways generating this voltage, consider circuit realizability d simplicity. Since the function resembles a capacity discharge, and at $t=\alpha$, $e=E_{max}$, and since a capacitor can be charged quickly and accurately to a given voltage by a cathode-follower circuit, assume a circuit configuration of the type shown in Fig. 4. (Other configurations may be found in Appendix III.) When the grid of the tube in Fig. 4 goes to E'_{max}, the capacitor C will charge to the value E_{max}. At $t=\alpha$, the voltage on the grid drops below zero and the charge on the capacitor begins to discharge through Z.

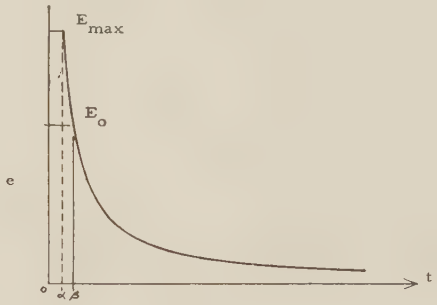

Fig. 3—The function $e=E_0\beta/t$.

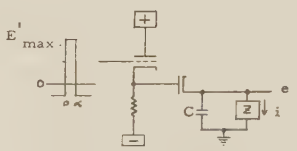

Fig. 4—Supposed Circuit.

The problem becomes one of determining Z such that (1) is satisfied. The equation is nonlinear. Therefore, some component must be nonlinear. Assume Z to be the nonlinear component, a function of e, $Z=Z(e)$. Write

$$e = \begin{cases} E_{max} - (1/C)\int i\,dt, & t \ge \alpha \\ E_{max}, & 0 \le t < \alpha \end{cases} \tag{2}$$

and

$$i = e/Z(e). \tag{3}$$

Substituting,

$$e = E_{max} - \frac{1}{C}\int \frac{e}{Z(e)}\,dt.$$

Differentiating and rearranging,

$$\frac{CZ(e)}{e}\,de = -\,dt. \tag{4}$$

Digress temporarily to our desired result; from (1),

$$e = \beta E_0/t \qquad t \ge \alpha$$

and hence

$$de/dt = -\,\beta E_0/t^2.$$

Eliminating t and rearranging,

$$\frac{\beta E_0}{e^2}\,de = -dt. \tag{5}$$

Now compare (5) with (4). If

$$Z(e) = \beta E_0/Ce, \tag{6}$$

then (4) becomes equal to (5), and the voltage e obeys (1).

It has been assumed that (6) is realizable. The necessary nonlinear load is a resistor which varies as the inverse of voltage across it.

Combining (3) and (6),

$$i = \frac{C}{\beta E_0}\,e^2. \tag{7}$$

Thus, $Z(e)$ is a nonlinear resistance whose current is proportional to the square of the voltage across it. The problem then becomes one of physically realizing (7).

Approximation of Nonlinear Load

It is necessary to approximate the nonlinear load described by (7), which may be normalized:

$$i/i_0 = (e/e_0)^2 \tag{8}$$

where

$$i_0 = (C/\beta E_0)e_0^2.$$

Eq. (8) shall be formed by the straight line approximation as shown in Fig. 5(a). The error obtained by this approximation is shown in Fig. 5(b). When $0 < e/e_0 < 1$, $i_\epsilon/i_0 = (e/e_0) - (e/e_0)^2$ and similarly for other values of e/e_0. A tabulation may be made as in Table I. An approximating circuit for the desired impedance function is shown in Fig. 6.

To determine R_0 (in Fig. 6) refer to (8) and Fig. 5. Assume that when E_0 is made a nominal value, a reasonable current is drawn by the load, *e.g.*, $i = 0.5$ ma when $E_0 = 50$ volts. Further, assume $n = 10$, so that $e_0 = 5$ volts; then from (8),

$$i_0 = i(e_0/e)^2 = 5\,\mu\text{amp}$$

and

$$R_0 = (e_0/i_0) = 1\ \text{M}\Omega. \tag{9}$$

The circuit which shall generate the function (1) ma be realized as shown in Fig. 7. The phantastron tim delay is adjusted for a time delay α as shown in Fig. The cathode follower V_2 is normally biased at cutoff an shall be used later as a hold circuit for sampling. V_3 i intended to provide a low impedance output. The volt

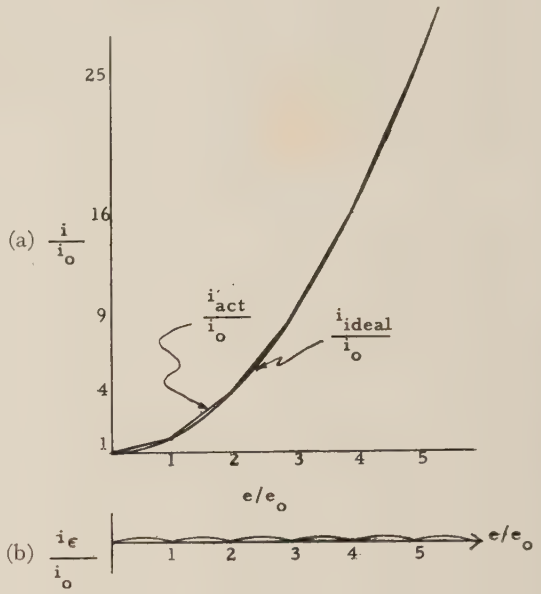

Fig. 5—(a) Straight line approximation o impedence function. (b) Error function.

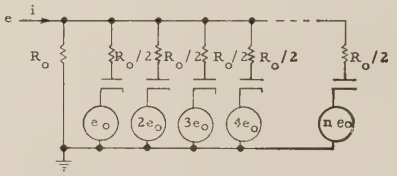

Fig. 6—Nonlinear impedance.

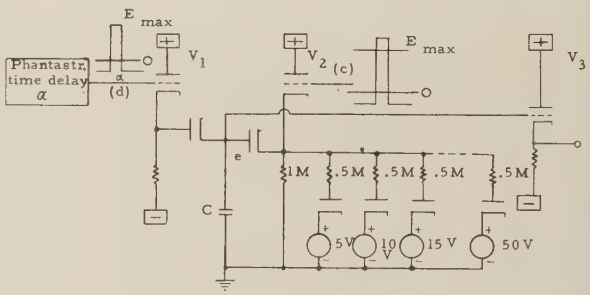

Fig. 7—$e = E_0\beta/t$ Function Generator.

TABLE I

Range	i_{act}/i_0	n	Error $(i_\epsilon/i_0) = (i_{act}/i_0) - (i_{ideal}/i_0)$
$0 < e/e_0 \leq 1$	e/e_0	1	$(e/e_0) - (e/e_0)^2$
$1 < e/e_0 \leq 2$	$e/e_0 + 2[(e/e_0) - 1]$	2	$3(e/e_0) - 2 - (e/e_0)^2$
$2 < e/e_0 \leq 3$	$e/e_0 + 2[(e/e_0) - 1] + 2[(e/e_0) - 2]$	3	$5(e/e_0) - 6 - (e/e_0)^2$
$3 < e/e_0 \leq 4$	$e/e_0 + 2[(e/e_0) - 1] + 2[(e/e_0) - 2] + 2[(e/e_0) - 3]$	4	$7(e/e_0 - 12 - (e/e_0)^2$
$n - 1 < e/e_0 \leq n$	$(e/e_0)(2n + 1) - n(n - 1)$	n	$(e/e_0)(2n + 1) - n(n - 1) - (e/e_0)^2$

ge e may be obtained in terms of the circuit constants. rom (2), (8), and (9), and the initial condition, $e=E_0$, t $t=\beta$, it can be shown by calculations similar to those erformed in the previous section, that

$$e = \begin{cases} \dfrac{R_0 C e_0}{t - \beta + CR_0 e_0/E_0}, & t \geq \alpha \\ E_{\max}, & 0 \leq t < \alpha. \end{cases} \tag{10}$$

t is clear from (10) that β must be set to

$$\beta = R_0 C e_0 / E_0 \tag{11}$$

(1) is to be satisfied.

omputation of e_{actual}.

Eq. (9) was calculated using the ideal nonlinear im- edance of (8). This does not include the error intro- uced by using the approximated segmented load. Fig. (b) shows the error in i/i_0 introduced by the approxi- nation. A correction to this error will have to be made ince its integral is cumulative and may become sig- ificantly large. Let us calculate e_{actual} and compare t with e_{ideal}.

$$e_{\text{act}} = E_{\max} - (1/C) \int i_{\text{act}} dt.$$

rom Table I,

$$i_{\text{act}} = i_0[(e/e_0)(2n+1) - n(n-1)];$$

hen,

$$e_{\text{act}} = E_{\max} - (i_0/C) \int (e/e_0)(2n+1)dt$$

$$+(i_0/C) \int n\,(n-1)\,dt.$$

he solution of this equation (see Appendix II) is

$$e_{\text{act}} = \frac{e_0 n(n-1)}{(2n+1)} + \left[E_0 - \frac{e_0 n(n-1)}{(2n+1)}\right]^{-(2n+1)(t-\beta)/R_0 C}$$

his equation indicates that e_{actual} is made up of a sum f constants and exponentials whose coefficients change ith n (as defined in Table I). When the initial condition hat $e=E_0$ when $t=\beta$ is imposed, and calculation for act is made at $t=10\beta$, then e_{act} is not exactly the same s e_{ideal}, as might be expected. This is because of the rror of Fig. 5(b). A correction to the actual curve must e made. A convenient method is to adjust for this rror by changing the value of e_0. This adjustment pro- ides adequate correction for the error introduced by pproximating the nonlinear load Z by straight line egments. It is adjusted to proper value along with two ther adjustments to make the error function as shown n Fig. 12 a minimum.

Block Diagram of PFAC and Circuit Details

The block diagram of the complete computer is shown in Fig. 8. The amplifier accepts an input of 0.1 volt rms or greater and drives the Schmitt Trigger which provides a square wave voltage as shown in Fig. 9(a). The phantastron time delay is triggered by the square wave as shown in Fig. 9(b). A phantastron circuit was used because precise time delay is necessary. The one-shot time delay provides a pulse as shown in Fig. 9(c). During the one-shot pulse, the $\beta E_0/t$ Function Generator (also Fig. 7) is clamped and the sampling is performed. The waveshape of Fig. 9(d) is generated by the stop gate shown in Fig. 8 and is limited to the voltage $E'_{\max}$. This waveshape is impressed on the input of the $\beta E_0/t$ Function Generator. The output of the latter is shown in Fig. 9(e). At proper time [Fig. 9(c)], the voltage of Fig. 9(e) is clamped, and is sampled as shown in Fig. 9(f) by the Sample Circuit and stored on a capacitor in the Hold Circuit, Fig. 9(g). The biased cathode follower

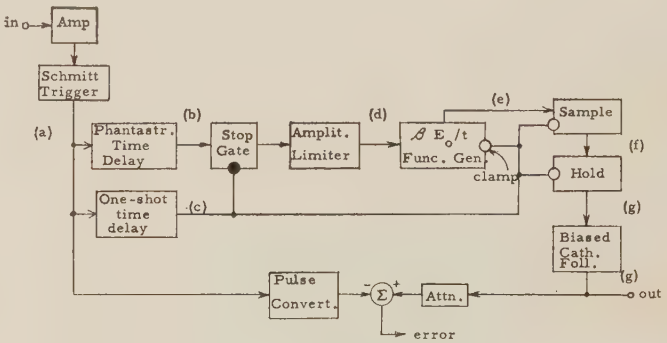

Fig. 8—Detailed block diagram of the FPAC.

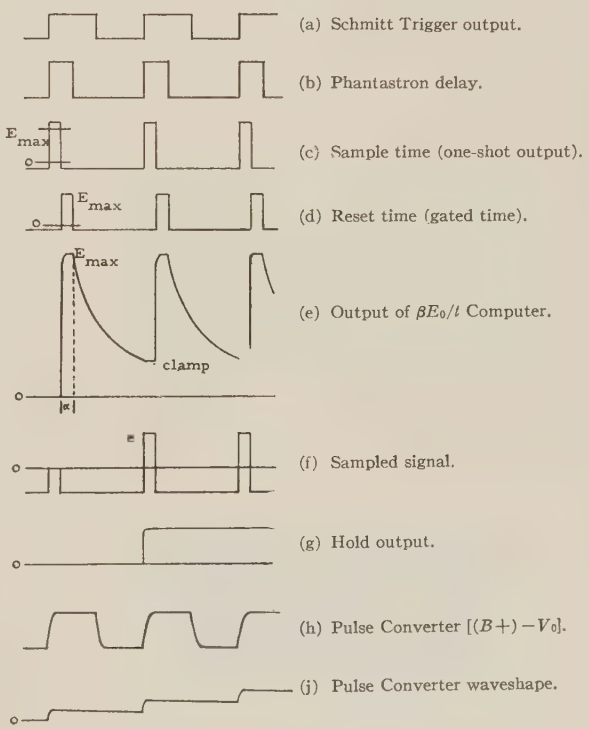

Fig. 9—Timing of the system.

provides a dc zero level control and low impedance output.

Accuracy of the system is checked by a standard Pulse Converter whose accuracy is nominally ± 0.1 per cent. Its output is subtracted from the output of the FPAC and the difference is proportional to the error in per cent of full scale. Fig. 9(h) and 9(j) show the waveshapes at points (h) and (j) in Fig. 11. Note the instantaneous response of Fig. 9(g) and the slow averaging response of Fig. 9(j). Note from Fig. 11 that a smoothing choke and capacitor follow point (j), causing still more delay.

Sample, Hold and Biased Cathode Follower Circuits

Fig. 10 shows the Sample, Hold and Biased Cathode Follower Circuits. The letters (e), (c), (f), and (g) correspond to the waveshapes similarly labeled in Fig. 9. The sampled voltage (f) is the smaller of the two voltages (e) and (c). The input cathode followers and diodes thus constitute the Sample Circuit. The Hold Circuit consists of the two triodes V_3 and V_4 connected cathode-to-plate, and the capacitor C_h. With signal Fig. 9(f) on the input to this circuit, the tubes are either both conducting or both cut off. When they are cut off, the capacitor C_h holds its charge. When a positive potential is present at (f), the upper tube acts as a cathode follower with the lower tube as a load, and the capacitor will charge or discharge to this potential. When (f) drops to cutoff level, the capacitor C_h holds its charge until a new level is impressed. The potential on the capacitor is read by cathode follower V_5. The potentiometer and Zener diode configuration provide a dc level adjustment without a corresponding change in gain. When no signal is present, the charge on C_h may drift to a negative value, so a diode is placed at the output to limit it to positive values only.

Pulse Converter

The pulse converter is a standard type used to convert a frequency to microamperes of current. The circuit is shown in Fig. 11. The square wave of Fig. 9(a) is impressed at (a) and is limited between $B+$ and V_0 at (h). The limited square wave is converted to a constant current by alternately charging and discharging C through the two diodes. The current may be determined:

$$i_c = \Delta q/\Delta t = C[(B+) - V_0]f$$

where f is the input frequency and $([B+]-V_0)$ is the peak-to-peak voltage across C. Since C, $B+$, and V_0 are constant, i_c is proportional to f.

If

$$C = 0.001\ \mu\text{fd},$$
$$B+ = 150\ \text{volts},$$
$$V_0 = 100\ \text{volts},$$
$$f = 1000\ \text{cps},$$

then

$$i = 50\mu\text{a}.$$

The voltage developed across the 200-Ω load is then 10 mv for 1000-cps input. If the output of the FPAC is applied to the 800-$k\Omega$ resistor at (g), a current i_g will flow as indicated in Fig. 11. If the constants are determined so that 40 volts output is obtained for 1-kc input, then $i_c = i_g$ and the error voltage across the 200 Ω will be zero. The error function may be obtained from this point with a microvoltmeter. If the latter is set for 100 μv full scale, then a full scale deviation will indicate a 1 per cent error. Error to ± 0.1 per cent accuracy may be measured by this method.

Adjustments

Final adjustments of the FPAC are made by adjusting the phantastron control for initial condition $e = E_0$ when $t = \beta$, and adjusting the zero control for $e = E_0/10$ when $t = 10\beta$. These two initial conditions occur when the frequency input is 1000 cps and 100 cps, respectively. A fixed adjustment on e_0 is made in order to minimize the error function of Fig. 12.

The FPAC was actually built with fourteen approximating sections so that a higher range of frequencies may be accommodated. The upper limit is actually 1500 cps, thus allowing good operation around 1 kc. The error function is plotted in per cent of $\frac{2}{3}$-full scale (which is at 1 kc).

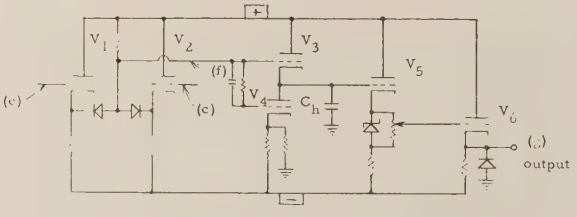

Fig. 10—Sample, Hold, and Biased Cathode Follower Circuits.

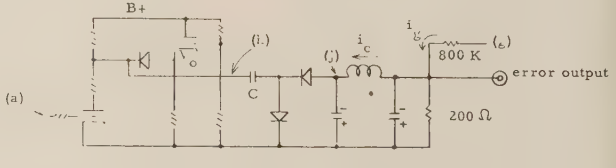

Fig. 11—Pulse Converter.

Fig. 12—Linearity of FPAC.

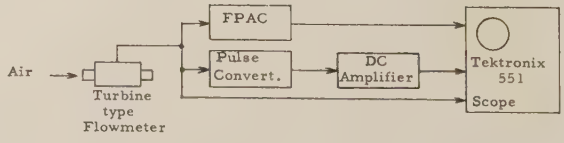

Fig. 13—Test setup of flowmeter response.

Results of Tests

Accuracy: Error function of Fig. 12 was obtained by plotting the difference between the FPAC and the Pulse Converter vs input frequency. The error is not more than ± 0.25 per cent of $\frac{2}{3}$-full scale (where full scale is 1500 cps) anywhere from 0 to 1500 cps.

Drift: Zero drift of the system is in the order of 0.5 per cent for normal long time measurement. This is caused mainly by variations in cathode emission of the four cathode followers cascaded in the Sample, Hold, and Biased Cathode Follower Circuits. This variation may be reduced by using regulated filaments.

Test Results: The FPAC was used to compute the average frequency for each cycle of a turbine-type flowmeter. Fig. 14 shows the output of the flowmeter (input to FPAC) on the lower trace, and the output of the FPAC on the upper trace, both as a function of time. The flowmeter was excited from zero flowrate by a sudden blowing into it. Note that each step represents a flowrate which is an average of the cycle just preceding it.

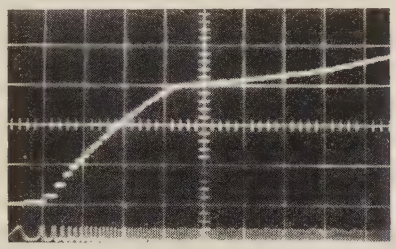

Fig. 14—FPAC readout of flowmeter. Horizontal, 20 msec/cmt Upper curve, output of FPAC, 250 cps/cm. Lower curve, output of flowmeter, 20 volts/cm.

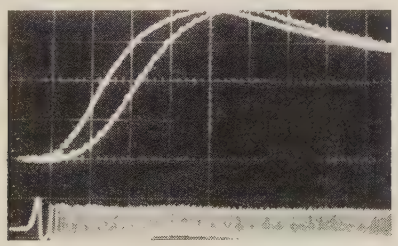

Fig. 15—FPAC vs Pulse Converter response. Horizontal, 50 msec/cm. Upper curve, output of FPAC, 400 cps/cm. Second curve, output of pulse converter, 400 cps/cm. Lower curve, output of flowmeter, 10 volts/cm.

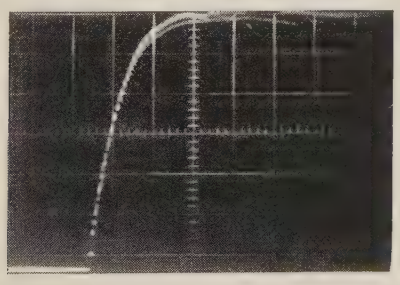

Fig. 16—FPAC readout of flowmeter. Air flow off axis. Horizontal, 200 msec/cm. Vertical, 125 cps/cm.

Fig. 15 shows the simultaneous outputs of the flowmeter on the lower trace, of the Pulse Converter amplified by a chopper stabilized amplifier on the middle trace, and of the FPAC on the upper trace. The test setup is shown in Fig. 13. Note the relatively poor response of the Pulse Converter and its inaccuracy in the transient state. The ripple seen on the trace is 60-cycle noise.

Fig. 16 shows the output of the FPAC when a turbine-type flowmeter whose blades are not evenly spaced was used. The blade misalignment causes a variation in period of the flowmeter output, which appears as a varying frequency. This causes the apparent double trace. Note that the apparent spacing of the blades changed at higher flowrates. The flow of air was injected at an angle off axis to the flowmeter. This may indicate chattering and/or change in axial position of the turbine.

Fig. 17 shows the sum of a 1-kc and a 60-cps sine wave and the corresponding variation of frequency as computed by the FPAC. The base line represents zero frequency for the upper trace. Fig. 18 shows the output of the FPAC when music from an FM receiver was impressed on its input. This photo is meant to illustrate its immediate response. Fig. 19 shows the front view of the FPAC unit.

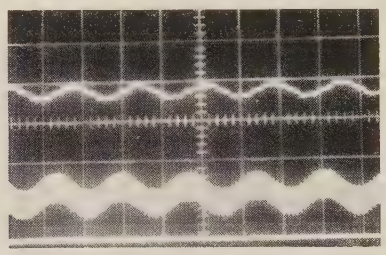

Fig. 17—FPAC readout of composite waveshape. Horizontal, 10 msec/cm. Vertical, 20 volts/cm.

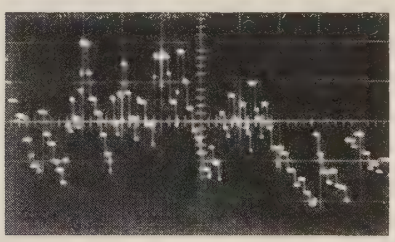

Fig. 18—FPAC Readout of music. Horizontal, 20 msec/cm. Vertical, 10 volts/cm.

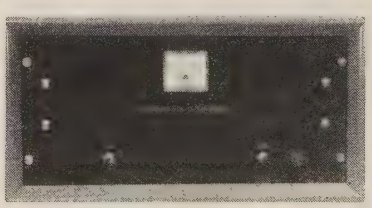

Fig. 19—FPAC unit.

Conclusions

The FPAC is a useful instrument for converting a varying frequency into a voltage proportional to the frequency without a time lag (as is necessarily obtained with an averaging type converter). The output of the computer is a dc level which is recorded immediately following the end of a cycle and is held at that level for the length of time of the next cycle. Accuracy of the system is better than ± 0.5 per cent of $\frac{2}{3}$-full scale.

It may be used to study frequency components of composite waveshapes.

It is a useful instrument (supplying substantial voltage) for use with turbine-type flowmeters, and may be used to determine their transient response.

Other Functions

Two other functions may be generated utilizing the k/t function generator. The function $\log_\epsilon (t)$, $t \geq \alpha$, may be generated by integrating k/t as shown in Fig. 20. Logarithmic time generators may be accomplished in other ways [4].

The function $1/t^2$, $t \geq \alpha$ may be generated by differentiating k/t as shown in Fig. 21. (See Berwin [5] for methods of differentiating.)

Appendix I

Digiflo

An instrument called the Digiflo, developed at Rocketdyne, accepts information from one (or two) turbine-type flowmeters, counts digitally the time interval of one (or several) complete revolutions of the flowmeter(s), and displays a number proportional to this time interval on two types of readouts: 1) Nixie type numerical indicating tubes (which may be photographed on a strip film camera (Fig. 24) and, 2) a coded waveshape current which drives a galvanometer in an oscillographic recorder. This instrument is presently being used at Rocketdyne.

Fig. 22 shows the block diagram of the Digiflo, Fig. 23 shows its coded output, and Fig. 24 shows its front view. (See Berwin [3].)

Appendix II

Calculation of e_{actual}

The equation of potential across the capacitor is

$$e_{\text{actual}} = E_{\max} - (1/C) \int i_{\text{actual}} dt.$$

From Table I,

$$i_{\text{act}} = i_0[(e/e_0)(2n+1) - n(n-1)],$$

$$e_{\text{act}} = E_{\max} - (1/C) \int i_0[(e/e_0)(2n+1)dt + \frac{1}{C} \int i_0 n(n-1)dt.$$

Let

$$P = i_0(2n+1)/Ce_0, \qquad Q = i_0 n(n-1)/C.$$

Then

$$e_{\text{act}} = E_{\max} - \int Pedt + \int Qdt,$$

$$\frac{de}{dt} = Q - Pe,$$

$$\frac{de}{Pe - Q} = -dt,$$

$$\frac{de}{e - Q/P} = -Pdt,$$

$$\log_\epsilon (e - Q/P) = -Pt + K_1,$$

$$e - Q/P = K_0 \epsilon^{-Pt},$$

$$e = (Q/P) + K_0 \epsilon^{-Pt}.$$

At

$$t = \beta, \qquad e = E_0.$$

$$E_0 = (Q/P) + K_0 \epsilon^{-P\beta},$$

$$K_0 = (E_0 - Q/P)\epsilon^{P\beta},$$

$$e_{\text{act}} = (Q/P) + (E_0 - Q/P)\epsilon^{-P(t-\beta)}.$$

Combining:

$$e_{\text{actual}} = \frac{e_0 n(n-1)}{(2n+1)} + \left[E_0 - \frac{e_0 n(n-1)}{(2n+1)} \right] \epsilon^{-(2n+1)(t-\beta)/R_0 C}.$$

Appendix III

Other Methods of Generating $e = k/t$

1) The function $y = k/t$, $t > 0$ may be realized with a multiplier as in Fig. 25.
2) The function $y = 1/(t+1)$ or $y = k/t$, $t > 0$ may also be realized with a squaring transfer function.

The equation of the analog computer of Fig. 26 is:

$$y^2 = -\dot{y},$$

$$\dot{y} + y^2 = 0.$$

Assume

$$v = 1/t;$$

then

$$\dot{y} = -1/t^2,$$

$$y^2 = 1/t^2;$$

substituting,

$$-1/(t^2) + 1/t^2 = 0;$$

therefore,

$$y = 1/t, \qquad t > 0$$

is a solution. $y = 1/(t+1)$ is also a solution. The squaring circuit may be a diode approximation cir-

cuit or a thyrite approximation circuit [6].

3) The function $1/(t+1)$ may be approximated to 0.36 per cent by the following equation:

$$\frac{1}{t+1} \approx \epsilon^{-0.375t} + 0.0673 - (0.476t + 0.0682)\epsilon^{-0.782t}.$$

This equation was obtained with an IBM computer program used at Rocketdyne, a Division of North American Aviation.

Fig. 20—Generation of $\log_\epsilon t$, $t>0$.

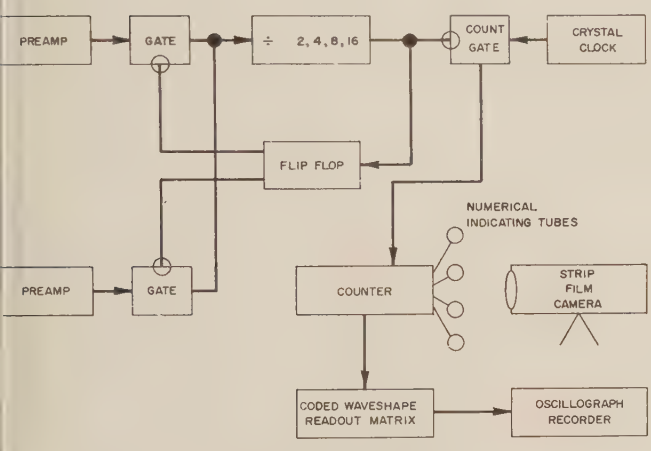

Fig. 22—Digiflo block diagram.

4) The function

$$\sum_{i=1}^{n} A_i e^{-K_i t}$$

may be used to generate the desired equation to good accuracy if n is large enough.

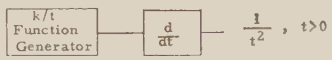

Fig. 21—Generation of $1/t^2$, $t>0$.

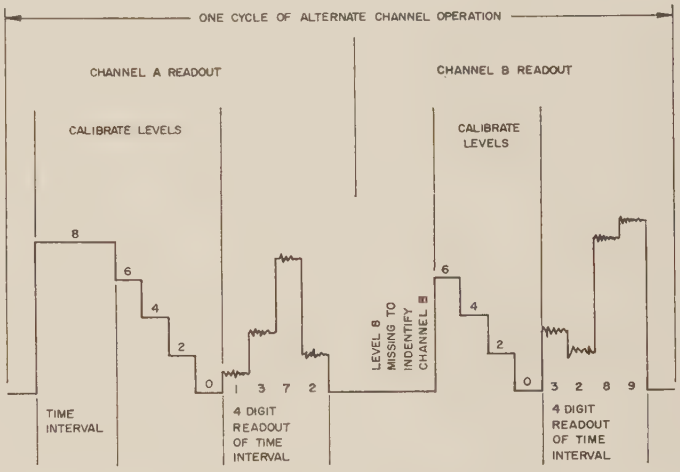

Fig. 23—Coded waveshape oscillograph output.

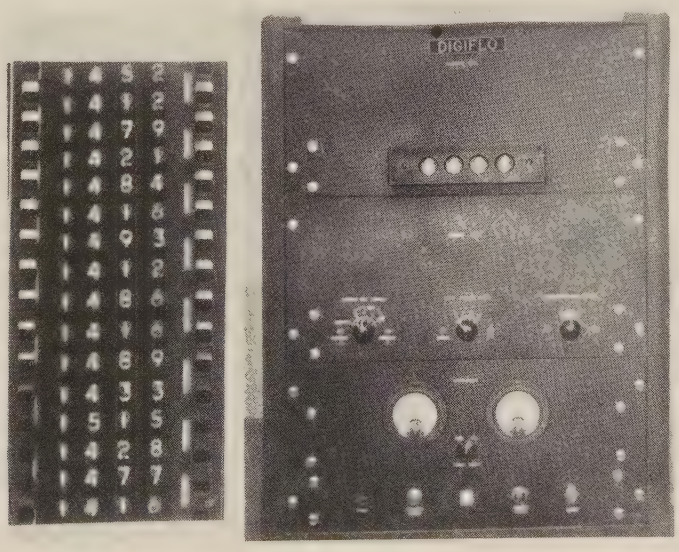

Fig. 24—Digiflo unit.

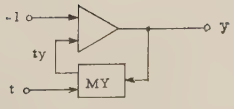

Fig. 25—Alternate k/t Function Generator using multiplier.

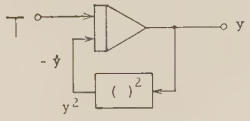

Fig. 26—Alternate k/t Function Generator using square circuit.

Appendix IV

Extending Transient Response of Turbine-Type Flowmeters Utilizing the FPAC

Since the output of the FPAC is proportional to the angular velocity of the flowmeter turbine, the difference in level of successive steps is proportional to the derivative of the angular velocity (*i.e.*, the acceleration term $\ddot{\theta}$). If the angular velocity of the turbine may be described by

$$I\ddot{\theta} + c\dot{\theta} = F(t, v)$$

where I is the moment of inertia, c is the frictional component, $F(t, v)$ is the force driving the turbine (a function of time and flowrate), then $F(t, v)$ may be computed simply by adding the proper proportions of $\dot{\theta}$ and $\ddot{\theta}$.

It would be an ideal situation if F were a linear function of flowrate v, for then the sum $I\ddot{\theta}+c\dot{\theta}$ would be truly proportional to $v(t)$. Unfortunately, this is not the case. However, the inertia term could be largely reduced if the $\ddot{\theta}$ term were used to supply or remove energy from the rotation of the turbine. For example, let us differentiate the output of the FPAC with a transfer function ($TS/TS+1$). Then pulses are obtained whose amplitudes are proportional to $\ddot{\theta}$. These pulses may be applied so that positive pulses will increase and negative pulses will decrease the angular velocity of the turbine. See Fig. 27 for a possible method to accomplish this. The system shows the output of the FPAC differentiated, amplified and separated so that energy is added if the signal is positive and subtracted if negative. The control circuitry is used to gate alternate pulses out so that alternate steps are functions of flowrate only, and the others are functions both of flow and the added or subtracted energy. Maximum achievable response time would be the time required for two blades to pass. If the blades are not perfectly aligned it may be necessary to consider sampling times of every revolution rather than every blade. Since $F(t, v)$ is generally a nonlinear function, it would probably be impossible to increase the transient response by this method to more than five times. Fig. 28 shows the schematic diagram of the FPAC

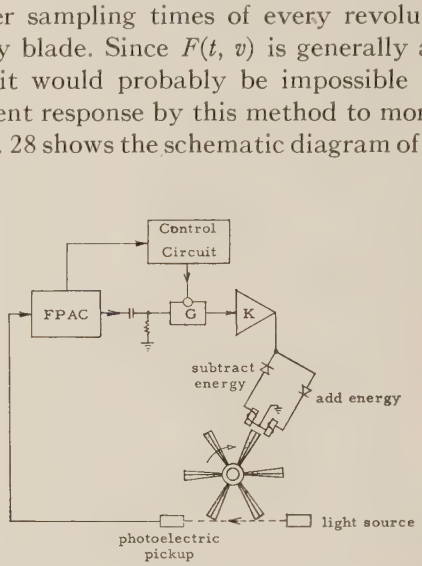

Fig. 27—Possible scheme to increase transient response of turbine-type flowmeters.

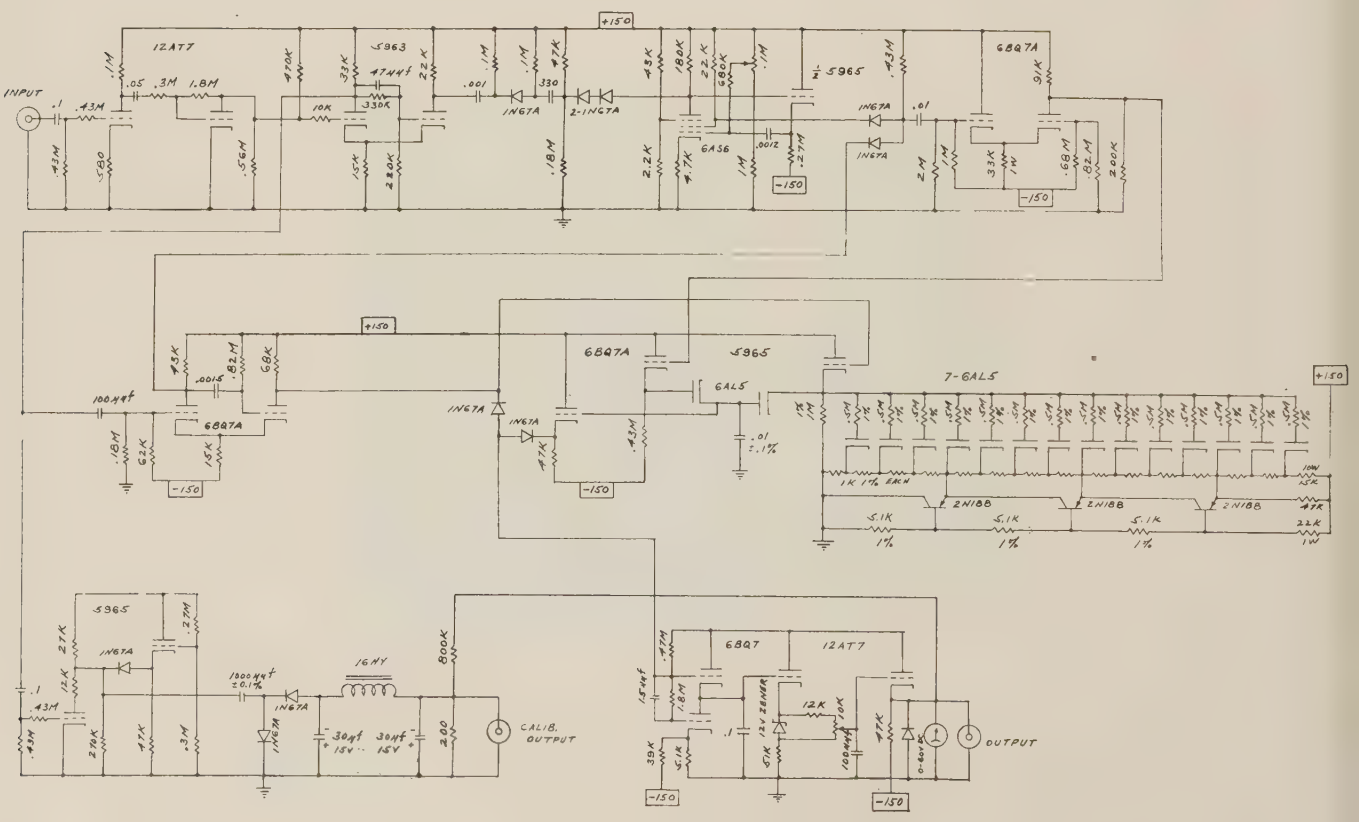

Fig. 28—Frequency-to-Period-to-Analog Computer.

Acknowledgment

The author wishes to express his appreciation to McGregor for his aid in the design, development, and nstruction of the Frequency-to-Period-to-Analog Com-ter; to Dr. F. F. Liu for his generous encouragement l guidance; to B. Dennis for the typing of this paper; M. Lee for his aid in photography; to H. Kasper for aid on the IBM 704 Digital Computer, in providing approximate solution for the k/t generator; and to esser Dynamics, A Division of Dresser Industries, ., and its many employees who helped in the develop-nt of the FPAC. Appreciation is also extended to Dr. J. Karplus of the Engineering Department, Uni-sity of California at Los Angeles, for his generous couragement and for sponsoring the writing of this per.

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[3] T. W. Berwin, *et al.*, "Technical Manual for the Digiflo-Research Report 57-47," Rocketdyne, Div. of NAA, Canoga Park, Calif., Internal Rept.; September 13, 1957.

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[6] L. D. Kovach and W. Comley, "Nonlinear transfer functions with thyrite," IRE Trans. on Electronic Computers, vol. EC-7, pp. 91–97; June, 1958.

Soviet Computer Technology—1959*

WILLIS H. WARE, *Editor*†

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Editor's Note—In contemplating the large amount of factual information, impressions and statistics which our delegation obtained in the two weeks we spent in the Soviet Union, it seemed advisable to me to present this material by topic, rather than to recite it in the chronological order of collection. Therefore, I have arranged the information under subject headings which appeared to be fitting. For this reason much of the text which follows represents my own wording, although each delegate may recognize phrases, sentences, or entire sections as being his own.

Because of the difference between the Roman and Cyrillic alphabet, the rendition of Russian names into English is subject to considerable variation. In this report I have attempted to use consistently the system of transliteration adopted by the United States Board on Geographic Names. In many instances the names of the Russians we met were available to us in both Cyrillic and the Roman alphabets; consequently, I have been able to verify the English rendition.

From visits of previous groups to the Soviet Union and from open literature sources, a certain amount of information about Russian computer development has gradually been accumulated. In order to maximize the effectiveness of our visit, the delegation made a strong effort not to investigate those areas which previously had been described. However, in order to make this report comprehensive within itself, I have taken the liberty of including a small amount of material from other sources. In particular, I have carried forward some of the information obtained by the Scott, Carr, Perlis, Robertson group which visited the Soviet Union in August, 1958.[1]

I have also checked a few other references in an effort to reduce conflicts between our information and that previously reported. It is hoped that this present report represents an essentially correct picture of the Soviet computer field as it is visible to visitors from the western world.

I have elected to report in a positive and definite style, but there is, of course, always a possibility that our factual material may be wrong. Among other things, the difficulty of communicating across a language barrier introduces uncertainties into the information.

—W. H. WARE

Summary—**The paper presents a factual account of the trip of the 1959 U. S. technical delegation in computers to the Soviet Union. It includes the itinerary, descriptions of specific Soviet computers, descriptions of certain computing centers, a discussion of Soviet computer-oriented education, and a description of current circuit and component development. In appendices are given the instruction repertoire of the URAL-I and the URAL-II machines, and an analysis of some magnetic cores. The paper is extensively illustrated and contains a bibliography of relevant Soviet documents.**

" . . . let us scientists continue to exchange information in friendship and peace."

—From a Russian toast

ORGANIZATION OF THE REPORT

THIS report has been divided into the following major sections:

Under "Organizations" is also included a certain amount of technical material of a miscellaneous nature which did not conveniently fit into other sections.

HISTORY OF THE DELEGATION

As a result of negotiations between the National Joint Computer Committee of the United States and the Academy of Sciences of the Soviet Union, an arrangement was concluded whereby a Russian delegation would visit this country in April of 1959, and an exchange American delegation would visit the Soviet Union in May of 1959. From April 19 to May 1 the Russian Delegation of seven visited approximately twelve factories, installations, research establishments, and other activities in the United States. The details of this group's itinerary and discussions have been published separately.[2]

Because the exchange had been arranged in the name of the National Joint Computer Committee as a representative of the computer societies of the United States, and because this was an exploratory trip, it was considered desirable that each of the three societies which comprise the National Joint Computer Committee, as well

* Manuscript received by the PGEC January 11, 1960.
† The RAND Corporation, Santa Monica, Calif. For the affiliations of the individual contributors, see the text.

[1] 1) "Status of Digital Computer and Data Processing Development in the Soviet Union," ONR Symp. Rept., ACR-37, Washington, D. C., November, 1958; and 2) Carr, J. W. and Perlis, A. J., "A visit to computation centers in the Soviety Union," *Commun. Assoc. for Comp. Mach.*, vol. 2, no. 6, pp. 8–20, 1959.

[2] E. M. Zaitzeff and M. M. Astrahan, "Russian Visit to U. S. Computers," *Commun. Assoc. for Comp. Mach.*, vol. 2, pp. 4–11; November, 1959. Also published in IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-8, pp. 489–497; December, 1959.

Name	*Affiliation*	*Representing*
Morton M. Astrahan	International Business Machines Corporation	Chairman of the delegation, Past Chairman of NJCC
Samuel N. Alexander	National Bureau of Standards	United States Government Agencies
Paul Armer	The RAND Corporation	Vice Chairman, NJCC
Lipman Bers	Institute of Mathematics, New York University	Interpreter
Harry H. Goode	University of Michigan, Bendix Systems Division	Chairman, NJCC
Harry D. Huskey	University of California	Vice Chairman, Association for Computing Machinery
Morris Rubinoff	Philco Corporation	Chairman, Computing Devices Committee, American Institute of Electrical Engineers
Willis H. Ware	The RAND Corporation	Chairman, Professional Group on Electronic Computers of the IRE

Members of the American Delegation

the NJCC itself, should be represented on the delegation. Six of the eight members of the delegation were therefore officers of the NJCC or its member societies, a representative of one of these. The two other positions were a representative of the many government departments which participated in the Russian visit to this country, and the interpreter for the group. The delegation was fortunate in having as a member Professor Lipman Bers of New York University; because of his personal stature as a mathematician and his fluent knowledge of Russian, we were able to obtain insight to Russian mathematics and social life.[3]

The members of the delegation are listed above. In addition, Mesdames Astrahan, Alexander, Armer, Huskey, and Ware accompanied the group. Each member of the delegation was financially supported by his own organization, or by a special grant from the government. Each wife paid her own way.

In an international exchange of this kind, it must be recognized that the difference in language is a serious barrier to the interchange of information. While the delegation had available the finest of interpreters, and while the translating in general was very good, in all cases the necessity of communicating across a language barrier hindered the free flow of ideas. It was apparent on many occasions that an inadvertent mistranslation of a single word changed the meaning of a key sentence, or misdirected the entire conversation. For this reason it was often necessary to rephrase and repeat a question several times in order to convey the proper implication. If information set forth in this report differs seriously from that reported elsewhere, there is, in addition to the difficulties imposed by the language difference, the possibility that some of the work in question is still experimental and therefore may have changed since an earlier report.

Fig. 1—Academician S. A. Lebedev.

Fig. 2—Technical guides. (*Left to right*) Aleksei Fedorov, Anna I. Martynova, Victor Zeidenberg.

Itinerary

The delegation arrived at Vnukovo Airport, Moscow, at approximately 10:35 P.M., Sunday, May 17, 1959. We were met by our host, Academician Sergei A. Lebedev (Fig. 1), and three members of his Institute: Victor K. Zeidenberg and Aleksei S. Fedorov, electrical engineers, and Miss Anna I. Martynova, a linguist (Fig. 2). The men were transported to the Hotel Sovetskaya by bus, while the women and Miss Martynova traveled to the hotel by car. It is appropriate at this point to express publicly the gratitude of the delegation to their host, and to the technical guides who were to make the stay of the delegation in Russia so pleasant, so cordial, and so memorable.

Monday, May 18

After the necessary but time-consuming exchange of dollars into rubles, the group traveled to Academician Lebedev's Institute of Precise Mechanics and Computing Techniques, which is located at 51 Leninskiy Prospekt in the southwest section of Moscow. In the morning the work of this Institute was discussed in a general fashion, and a visit was made to the BESM-I

[3] Professor Bers used the occasion to establish contact with mathematicians in the Soviet Union. A copy of his report can be obtained by writing to him.

installation. Following lunch we visited laboratories working on the following topics:

1) Transistor parameters,
2) Transistor circuits,
3) Core materials,
4) Core switching time,
5) Thin magnetic films,
6) Magnetic circuits.

We met or spoke with the following people:

I. S. Mukhin, Deputy Director of the Institute;
V. A. Melnikov, Engineer;
V. V. Bardizh, Engineer;
P. P. Golovistikov;
Yu. I. Sharapov;
——— Vasilev.

Tuesday, May 19

The group visited the Moscow Computing Center of the Soviet Academy of Sciences. This organization and part of the Steklov Institute for Mathematics[4] share a building at

Akademichesky Proezd
Dom No. 28
Moscow V-134.

We discussed the work of this organization and visited the URAL-I, the STRELA-III,[5] and the BESM-II installations. We met or spoke with the following people (Fig. 3):

A. A. Dorodnitsyn, Director of the Computing Center, Aerodynamicist;
V. A. Ditkin, Deputy Director of the Computing Center;
V. M. Kuzochkin, Head, Programming Laboratory;
A. P. Yershov, Head, Theoretical Programming Department;
V. P. Smizyagin, Chief Engineer;
P. T. Chushkin, Scientific Staff Worker in Aerodynamics and Gas Dynamics.

[4] It is frequent in Russia for an organization to be named in honor of an important personage. This is done by coupling the name of the institute to the name of the person with the word "imeni" which means "in the name of." The proper name of the Steklov Institute is, therefore, the Institute of Mathematics imeni V. A. Steklov. Frefiuently such long titles are shortened by using the man's name to describe the institute. Another example is that of Moscow State University imeni M. V. Lomonosov, which is frequently called simply Moscow State University or, sometimes, Lomonosov University. On other occasions an institute is referred to by the title of its Director. For example, the Institute of Precise Mechanics and Computing Techniques is sometimes referred to as Lebedev's Institute, although this particular case creates confusion because of the Institute of Physics imeni P. N. Lebedev.

[5] Occasional references in the literature have suggested that different versions of the STRELA machine exist. For instance, in *Datamation*, vol. 5, no. 4, p. 14, reference is made to the STRELA-III machine installed at the Academy Computing Center. Other references in the literature mention a STRELA-I, a STRELA-II and a STRELA-IV.

Fig. 3—Personnel at the Academy of Sciences Computer Cente (*Top, left to right*) A. A. Dorodnitsyn, A. S. Fedorov, V. I Smizyagin, A. P. Yershov, P. T. Chuskin. (*Bottom, left to righ* A. A. Dorodnitsyn, V. A. Ditkin, V. M. Kuzochkin, A. P. Yersho

Following lunch the group split into two parts. Ber Goode, Rubinoff, and Ware discussed with G. E Linkovsky his theory of the memory function in th human brain. The rest of the group visited and hear described the BESM-II.

Wednesday, May 20

In the morning the group visited the Institute fo Scientific Information in Moscow, located at Baltii skaya Ulitsa 14, and discussed its work on informatio storage, retrieval, and dissemination. We discussed a some length plans for automating these functions wit Professor L. I. Gutenmakher. We met or talked with th following people:

Professor A. I. Mikhailov, Director, All-Union In stitute of Scientific and Technical Informatio (VINITI);
Professor L. I. Gutenmakher, Head, Laborator for Electro-Modeling;
B. M. Rakhov;
——— Cherny.

In the afternoon the group reconvened at the Insti tute for Precise Mechanics for a discussion of languag translation. We met or talked with the following people

I. S. Mukhin, Deputy Director of the Institute i charge of language translation research;
V. V. Ivanov,[6] Head, Language Translation group
——— Korder, Assistant to Mukhin;

[6] Affiliation uncertain. He may be a general consultant to IPMC and also affiliated with The Institute of Language Studies of th Academy of Sciences, with the Committee for Applied Linguistics the Academy of Sciences, with Moscow State University, and wit the Institute of Pedagogical Sciences.

V. V. Parshum,[7] German to Russian translation;
G. A. Volchek, Japanese to Russian translation;
(Mrs.) T. M. Nikolayeva, Russian to other languages translation;
V. A. Voronin, Chinese to Russian translation;
——— Bobitsky,[8] Russian to other languages translation;
(Miss) A. I. Martynova, English analysis (one of our technical guides and the principal Soviet interpreter);
(Mrs.) G. P. Zelenkevich, Mathematician;
N. L. Korolev, Mathematician;
M. B. Yefimov, Japanese to Russian translation.

hursday, May 21

The group again split. Goode and Rubinoff visited the stitute for Automation and Telemechanics at 15A alanchevskaya Ul., Moscow 15. They discussed ana- g computing devices and developments in switching eory and remote control. They met or spoke with:

Boris S. Sotskov, Deputy Director;
A. M. Gavrilov, Senior Professor;
B. Y. Kogan, Engineer;
——— Petrovskiy, Secretary of the Institute;
——— Parkhomenko;
——— Gruenberger, Staff Engineer;
G. K. Moskatov.

he rest of the group visited the Lomonosov campus of oscow State University and its computing center. The ork of this computing center was discussed and the TRELA and SETUN installations were visited and escribed. We met or spoke with the following:

Academician S. L. Sobolev, Head, Computing Chair, MSU;
I. S. Berezin, Director of the Computing Center;
M. R. Shura-Bura, Professor of Numerical Analysis;
N. P. Zhidkov, Professor and Senior Scientist;
N. P. Brusenzov, Chief Engineer of the SETUN machine.

The Director of Moscow State University was host to ie delegation at a formal luncheon in the university. t this time we met or spoke with the following people:

Academician I. G. Petrovskiy, Rector, Moscow State University;
N. P. Zhidkov, Professor and Senior Scientist;
Academician I. M. Gelfand, Professor of Mathematics, MSU;
Academician I. R. Shafarevitch, Professor of Mathematics, MSU;
Academician S. L. Sobolev, Head, Computing Chair, MSU;
Ye. M. Landis;
I. S. Berezin, Director Computing Center, MSU;
——— Nikiforov, Head, Foreign Department, MSU;
M. R. Shura-Bura, Professor of Numerical Analysis.

The part of the delegation which had visited the Institute for Automation and Telemechanics arrived in time to join the luncheon.

In the evening, Academician and Madame Lebedev were host to the delegation at their Moscow apartment. Following an outstanding example of Russian hospitality, the group departed on the overnight Red Arrow Express for Leningrad.

Friday, May 22

The delegation visited the Computing Center of Leningrad University which is physically located in the building of the Institute of Mathematics and Mechanics. The address is:

Fak. Vychislitel'nyy Tsentr
Matiko-Mekhanicheskiy
10 Pinikh D. 33
Leningrad, B-178 B. O.

We discussed at some length the curriculum for training of computer-oriented mathematicians. We later visited installations of the URAL-I, the EV-80, the MN-M and the MPT-9 analog machines. We met or spoke with the following people:

Professor S. V. Vallander, Director, Institute of Mathematics and Mechanics, Hydrodynamicist;
M. K. Gavurin, Deputy Director, Computing Center, Professor in the Theory of Functions;
A. N. Baluyev, Second Deputy Director, Computing Center;
——— Bulovsky, Research Assistant, Programmer, Statistician;
S. Ya. Fitialov, Research Associate, Programmer interested in Mathematics and Linguistics;
Professor D. K. Fadeyev;
Mme. V. H. Fadeyeva;
Mme. O. A. Ladyzhenskaya, Mathematician, interested in partial differential equations;
Professor S. G. Mikhlin, Mathematician, interested in integral equations;
Professor M. L. Tsetlin, Logician, interested in the Theory of Automata.

Saturday, May 23

The group visited the former summer palace of the Czars at Peterdvorets. In the afternoon we visited other historical sights around Leningrad. Saturday evening we returned by overnight express to Moscow.

[7] Spelling uncertain. May be Parshin.
[8] Spelling uncertain. May be Barbitsky.

Sunday, May 24

In the afternoon the group visited the Kremlin and, in addition to the more usual tourist sights, were privileged to have special permission to see the Great Palace of the Kremlin.

Monday, May 25

The group split into three sections. Armer met privately with Yershov to discuss matters of programming and operation of the Academy Computing Center. Ware met with a group of BESM engineers to discuss general matters related to design philosophy, reliability, components and so forth. He spoke with:

V. V. Kobelev,
V. S. Burtzev,
V. Ya. Alekseyev,
M. V. Tyapkin,
V. N. Laut.

The rest of the group left by plane for Penza to inspect the computing machine factory and to see the URAL-I machine in production. (Address: Vavod Schetno Analicheskikh Mashin, Penza.) They also saw the prototype of the URAL-II and learned its characteristics. They met or spoke with the following:

V. A. Matkin, General Manager;
V. A. Buanov, Deputy General Manager;
V. M. Stepanov, Engineer of Soviet Production;
A. M. Ivanov, Engineer of Regional Production;
A. D. Pavlov, Engineer;
B. I. Rameyev, Chief Design Engineer.

Tuesday, May 26

The group reconvened at the IPMCT for a round-table discussion. Such topics were discussed as digital differential analyzers, the relation between digital differential analyzer and general-purpose machines, the inter-connection of computing machines by communication networks, reliability of transistors, machine organization, etc. The people whom we met and spoke with are as follows:

——— Bachin,
E. F. Berezhnoy,
P. P. Golovistikov,
N. N. Chentsov,[9]
Yu. I. Sharapov,
S. G. Kalashnikov,[9]
K. S. Neslukhovskiy,
M. V. Tyapkin,
V. N. Laut,
——— Kuzmichev,
O. K. Shcherbakov,
V. Ya. Alekseyev,
——— Galskiy,
P. S. Oraevskiy,
——— Pitkevich,
V. V. Kobelev,
V. V. Bardizh.

[9] Initials uncertain.

Wednesday, May 27

In the morning and early afternoon the group visited a facility of the Moscow Computing Machine factory where we saw and heard described a hitherto undisclosed machine, the M-20. We met or spoke with the following people:

I. I. Konyakhin, Director of the facility;
M. K. Sulim;
——— Kondramov;
A. A. Solovev.

We again were treated to Russian hospitality with a sumptuous luncheon served in the Director's office.

Late in the afternoon the group flew to Kiev where they were met by a party from the Computing Center of the Ukrainian Academy of Sciences and driven to the Hotel Ukraina.

Thursday, May 28

The group visited the Kiev Computing Center of the Ukrainian Academy of Sciences located at:

Bolshaya Kitayezskaya 115
Kiev 28.

We discussed the work of the computing center and learned of some of their automatic programming work. We also visited and had described the KIEV computing machine, a special purpose analog computing machine, the SESM computer, and some experimental work in character recognition.

We saw or spoke with the following people:

V. M. Glushkov, Director, Computing Center, Academy of Science, Ukrainian SSR;
B. N. Malinovskiy, Proxy of the Director of Scientific Matters, Candidate of Technical Sciences;
A. I. Kondalyev, Scientific Secretary, Candidate of Technical Sciences;
G. E. Pukhov, Head of Department, Doctor of Technical Sciences;
L. N. Dashevskiy, Head of the Department (in charge of KIEV machine), Candidate of Technical Sciences;
Yu. V. Blagoveshchenskiy, Chief Scientific Associate, Candidate of Technical Sciences;
V. N. Ostapenko, Chief Scientific Associate, Candidate of Physico-Mathematic Sciences;
E. L. Yushchenko, Head of Department, Candidate of Physico-Mathematic Sciences;
Z. L. Rabinovich, Chief Scientific Associate, Candidate of Technical Sciences;

V. E. Shamanskiy, Head of Department, Candidate of Physico-Mathematic Sciences;
I. T. Parkhomenko, Chief Engineer (acting);
Yu. T. Mitulinskiy, Chief Engineer;
V. A. Kovalevskiy, Chief Scientific Associate, Candate of Technical Sciences;
V. I. Shurikhin, Chief Scientific Associate, Candidate of Technical Sciences;
N. N. Pavlov, Junior Scientific Associate, Candidate of Technical Sciences;
R. Ya. Chernyakh, Candidate of Technical Sciences;
V. V. Kraynitskiy, Chief of Department.

That evening we were the guests of Dr. Glushkov and other members of his organization at the Dynamo Restaurant in Stadium Park in Kiev.

Friday, May 29

The group returned by air to Moscow and spent the balance of the day preparing for departure.

That evening a farewell dinner was given for the delegates and their wives by Academician and Madame Lebedev at the Hotel Ukraina. In addition to the Lebedevs, the U. S. delegates and their wives, the technical guides and interpreters, also present were Professor Ditkin; Mr. Bardizh; Mr. V. S. Petrov, Director of the Moscow Computing Machine plant; and Mr. P. S. Oraevskiy, Staff of the Presidium Office of the USSR Academy of Sciences.

Saturday, May 30

The delegation departed from Vnukovo Airport, Moscow, via Aeroflot TU-104A Jets, some of the party proceeding to Copenhagen and the remainder to Amsterdam.

It is interesting to note that the only locations where the group was requested not to take photographs were the computing machine factories at Penza and at Moscow, the Institute of Automation and Telemechanics, airports, and coastal locations. At no time was there any restriction on making notes. A number of the photographs which were taken by various members of the group have been included with this report, in order to illustrate some of the machines seen and some of the new developments in Soviet computer technology.

In judging the quality of the pictures included in this report, bear in mind that conditions for photography were not always ideal. Some of the illustrations are reproduced from 35-mm color slides, and others are reproduced from black and white negatives taken by subminiature cameras, or from black and white prints. In some cases a picture is an enlargement of a portion of the original. It is hoped that the illustrations, though not always technically excellent, will contribute to a sense of familiarity with Soviet personnel, places, and machines.

Organizations

The Institute of Precise Mechanics and Computing Techniques

This was the host Institute to our delegation (Fig. 4). Prior to coming to this Institute as its Director, Academician Lebedev was at the Kiev Academy of Sciences and was responsible there for the construction of the MESM digital computing machine, said by the Kiev workers to be the first electronic computing machine in continental Europe. Subsequent to his coming to Moscow as Director of IPMCT, Academician Lebedev has been responsible for the development of the BESM-I, BESM-II, and other machines.

Fig. 4— The Institute of Precise Mechanics and Computer Techniques. Inset: the Institute Address Emblem.

The building itself is reminiscent more of an academic building than an industrial building. It is equipped with the usual offices and laboratory facilities as well as a large lecture hall. Within an office the decor tends to be ornate; the entrance door is frequently padded on both sides with what appeared to be leather, and heavy drapery usually hung across the doorway and at the windows. The ceiling height was somewhat higher than that of contemporary American construction, but we felt in general that working conditions in the offices and in the laboratories were good. There appeared to be an adequate amount of room and the workers were comfortably supplied with material and equipment. The building was constructed in 1951. Many things testified to the steady and heavy usage which it has received. In Russian tradition, the floor is parqueted and of unfinished oak. As in nearly every building, there are two sets of permanent windows for weather protection.

Most of the discussions which took place at IPMCT fit naturally into other parts of this report; however, the discussion of the second Tuesday afternoon was so heterogeneous that it is included here. This discussion had been suggested by Lebedev in order to give a large number of his staff an opportunity to exchange information with the delegation. During a discussion of digital differential analyzers it was indicated that the interest at IPMCT in this device was as an adjunct to a general-purpose digital computer. The opinion was expressed

that the DDA might be a very useful device to process input information for certain kinds of problems to be handled by a general-purpose machine, *e.g.*, partial differential equations. Such a capability might be added to the BESM-II. They were familiar with the American literature on this subject, and asked by name about the TRICE machine. Other unnamed institutes in Russia are actively engaged in designing and constructing digital differential analyzers.

In a discussion about the structure of machine instructions, Lebedev commented that they had in the past preferred 3-address instructions; but since larger stores and longer addresses have appeared, they now tend toward single-address instructions because the word length for a 3-address format becomes too long for the precision needed in the arithmetic. They have made an analysis of a number of problems which shows that most machine operations are 2-address in nature; the opinion was expressed that a 2-address instruction format might be an eventual and reasonable compromise.

The Institute of Automation and Telemechanics is considering combined analog-digital computing systems for some of their problems. It has been their experience that unacceptable errors accumulate when large problems are attempted with an analog computer. Because of higher unit costs for digital equipment, more money is available for it than for analog equipment.

IPMCT hopes to improve the speed and logical design of their machines by using special vacuum tube structures for binary adders and switching. They feel that ferrites are not fast enough for such special structures, nor do semiconductors appear to have a place for this purpose. Low-temperature, thin-film magnetic devices are being seriously considered for more sophisticated, multiple-element switching devices.

There seemed to be general agreement between the Russian group and the delegation on the techniques for faster machines. Suggestions included: simultaneous operations such as overlapping the fetch of the next instruction with the execution of the present instruction; making slower units work in parallel to feed faster units; accelerating fast units by improved circuit techniques, or more sophisticated logical devices; inclusion of new multiple operation instructions in the machine repertoire; increasing the size and speed of the working store. In connection with the size of the working store, it was felt by the Russians that so far as scientific calculations are concerned, a large store may help programming efficiency more than it contributes to increased machine speed.

We were asked about transistor reliability in our machines and we in turn inquired about their comparable experience. They referred to a working experimental transistor machine elsewhere in Moscow which contained several thousand transistors. Their life experience indicated that a few tens of transistor failures had occurred in a few months of operation, of perhaps five hours per day. They expect to publish details of this machine soon.

They have experimented somewhat with computing machines connected to communication lines, but this is not a regular technique. They felt that machines coupled by communication networks is not a technique to be studied of itself. The details of each application would depend on the problem to be solved. Lebedev maintained strongly that it does not make sense to share a problem between several machines linked by communication channels, although he did admit that for special purposes it is reasonable to transmit data over lines to the machine.

The Moscow Computing Center of the Academy of Sciences

The Computing Center of the Academy of Sciences was formerly a part of IPMCT. As it expanded, it moved to its own building, of which it now occupies the first and third floors (Fig. 5). The second floor is occupied by mathematicians of the Steklov Institute.

Fig. 5—Moscow Computing Center of the Academy of Sciences.

About 95 per cent of the machine hours at the computing center are devoted to scientific and technical work. In the course of a year about 100 different institutes put problems on the machines. About half of the machine time is used by computing center personnel themselves, and outside institutes use the other half. The outside customers all do their own programming, and, for the most part, are physicists and engineers who have received training in programming from the computing center. At the moment there are approximately 300 people in the computing center; but it was estimated that 1000 people would be required to do all of the programming for the work being done on their machines—the STRELA, the URAL-I, the BESM-I, and the BESM-II. Apparently the computing center still makes extensive use of the BESM-I, even though it is located in the nearby IPMCT building. It appears that BESM-II, although just finished, provides production time. A typical problem was said to be approximately 500 3-address instructions and would take about ten days to be programmed and coded. In such a problem, ten programming errors would be regarded as a poor showing.

The general mode of operation is as follows. Programmers from the outside who come to the computing center with a problem apply to the scientific secretary of the computing center. He assigns someone from the computing center to provide any assistance needed by

he outside programmer. In general, an operator is provided for each machine, and only programmers with pecific permission can operate the machine personally. Normally a programmer can expect only one code check pass per day at a machine; with a very high priority he might get two or three passes.

A programmer is required to submit his manuscript in ink. Examples of manuscripts which we saw indicated that often a manuscript is written in pencil until it is thought to be correct, and then redone in ink. The manuscript is then key-punched twice, and the two decks compared, before being sent to the machine. The output cards are handled on an off-line printer.

In general there is a reasonable amount of cooperation between the machine designers and the programmers, with the programmers taking a considerable part in the design of machines. However, their experience has been that in most organizations which received a machine a local group of engineers was willing and eager to change the character of the machine. In this connection it was observed that the interchange of routines for STRELA machines was virtually impossible because no two of the machines were alike. It was also suggested that the same situation prevails for the URAL-I machines. As a result, user organizations do not exist for the URAL-I or for STRELA. Dorodnitsyn thought it was too early to standardize language for the whole of the Soviet Union on a specific machine. He suggested that they plan to design a large number of machines and to construct enough of each to provide adequate operating experience. Perhaps in five years a decision would then be made as to which machine and which language should be chosen for standardization.

The computing center's responsibility is largely for scientific and engineering calculations. A government scientific technical committee has recently been formed and will be responsible for commercial applications of computers. Any special machine required for this work will presumably be developed by laboratories or institutes connected with industry, rather than those connected with the Academy of Sciences.

The Moscow State University imeni V. M. Lomonosov, Department of Mathematics

Mathematics at Moscow State University (Fig. 6) is taught in the Faculty (*i.e.*, department) of Mathematics and Mechanics. Most other Russian universities have a joint Faculty of Mathematics, Mechanics, and Physics. The Dean of the Mathematics and Mechanics Faculty is now the fluid-dynamicist N. A. Slezkin, who succeeded Kolmogorov. A Mathematics section of the Faculty comprises eleven subdepartments or "chairs," each of which was originally occupied by a single professor, but now includes several people. These chairs and people in charge are as follows:

Analysis: N. V. Yefimov[9] (This chair is the service part of the department. It is responsible for the teaching of mathematics to non-mathematicians throughout the university);

Fig. 6—Moscow State University. (*Top*) Front view, (*bottom*) rear view.

Geometry and Topology: P. S. Aleksandrov;
Differential Geometry: S. P. Finikov;
Differential Equations: I. G. Petrovskiy;
Probability and Statistics: A. N. Kolmogorov;
Number Theory and History of Mathematics: I. M. Gelfand;
Function Theory and Functional Analysis: D. Ye. Menshov;
Logic: A. A. Markov;
Computational Mathematics: S. L. Sobolev. (This is the Russian equivalent of Numerical Analysis.)

During the first two years, a student of mathematics is not attached to a given chair but takes a standard set of courses. After two years he must decide on his specialization. In making this decision he is helped by general expository lectures given by a representative of each chair. The above list of chairs indicates only a partial picture of the overwhelming concentration of mathematical talent at Moscow University. For instance, the Chair of Function Theory and Functional Analysis contains, in addition to its leader, such people as I. M. Gelfand, G. Ye. Shilov, P. A. Raykov,[9] and others. L. S. Pontryagin and M. M. Postnikov[9] are attached to the Topology Chair. The mathematics group at Moscow State University is equaled only at one or two other places in the world.

In addition to the strong mathematics department at Moscow State University, there are prominent mathematicians connected with other institutions of higher learning in the Moscow area. There are also people whose primary assignment is elsewhere, but who also teach at MSU; for instance, S. N. Mergelyan, director of a computing center in Yerevan, the capital of Soviet

Armenia, and some members of the Novosibirsk branch of the Academy of Sciences.

The mathematicians in Moscow appear to be very well informed on the work in the United States. They publish a separate journal for translations of foreign papers, and large numbers of foreign scientific books are translated into Russian and published.

Computing Center

The Computing Center organizationally is within the Chair of Computing, although it appears to be independent in the sense that it has its own separate funds and its own scientific council of representatives from other Chairs in the University. Originally the Computing Center consisted only of the Chair of Computational Mathematics, of which Sobolev is still the head. In December, 1956 they received a STRELA machine which was characterized as the first computer that had been built by Soviet industry. The Center now includes two laboratories devoted to different aspects of computational mathematics. One of these is a programming laboratory which is concerned with numerical solutions of applied problems and includes several groups:

Electrodynamics: A. N. Tikhonov;
Numerical Weather Prediction: I. A. Kobel;
Gasdynamics: G. I. Petrov;[9]
Automatic Programming: M. R. Shura-Bura.

Shura-Bura's group is also responsible for the Theory of Programming, and for providing computing services to other people with problems. They charge 600 rubles per hour for the STRELA,[10] although the group sometimes does work for industry at no charge, provided it is sufficiently interesting.

The second laboratory at the Center has just recently been formed and concerns itself solely with numerical analysis. It is headed by N. P. Zhidkov.

The Computing Center is responsible for training all mathematicians who are specializing in computers. Forty per cent of the mathematics students at Moscow State University are specializing in numerical analysis, but every mathematician must take at least one year of numerical analysis and computing mathematics. The university provides its own maintenance engineers for their machines.

The university expects to obtain a large, new, industrially-produced machine in a year or two. Future users of this new machine have agreed not to modify it in order that an effective interchange of routines might be accomplished. At the moment an informal users' organization of 20 members already exists for it.

The lack of an alpha-numeric printer is something of a nuisance to the Computing Center, and they hoped that such printers will be available for their machines in the reasonable future.

The Institute of Automation and Telemechanics

It appears that most analog computer developments take place at this Institute. It does work not only in the development of specific analog computing devices, but also in the field of remote control devices, design of relay networks, and the design of specific devices to assist in analyzing and synthesizing relay networks. We were shown the following devices:

1) A chopper-stabilized operational amplifier whose drift was 13 mv over 2 hours, or 66 mv over 8 hours. It consisted of an ac amplifier with a 100-cycle to 100-kc pass band in parallel with a chopper-stabilized dc amplifier having a pass band from zero to 100 cycles.

2) Function generators. One type was the conventional diode-function box, sometimes used in the input or in the feedback position of an operational amplifier. A second type was that with a drum which has on its surface a wire shaped to the desired function. This technique is familiar in the United States.

3) Limiters. Two types were shown with the characteristics given in Fig. 7.

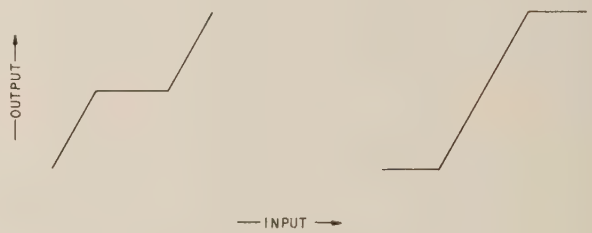


Fig. 7—Limiter characteristics.

4) A three-dimensional flight table with a 5-cps response, and amplitudes up to 6 degrees on each axis.

5) An analyzer machine. This was developed by Gavrilov and Parkhomenko. It is intended to examine the performance of a given relay circuit to see whether it agrees with a previous analysis. It consists of two large cabinets, of which the left one is a series of jacks, plugs, and wires for simulating a desired test circuit of up to 20 variables. The right-hand box contains 480 three-way switches arranged in 20 columns of 24 each. The 20 rows represent the 20 variables of the test circuits and the 24 columns represent 24 time steps. These switches are set to represent the condition of each variable at each switching time. A step switch sequentially progresses through the 24 time periods, in each of which the test in the left-hand box is compared to the state set by switches in the right-hand box. The machine stops if these do not compare identically, and the designer can then study the situation to locate the design error. At each such stop the machine also punches out a

[10] The ruble per dollar ratio is artificial in the sense that there is no free market exchange of rubles for dollars. For a tourist or visitor within Russia the exchange rate is set by the Government at ten rubles to the dollar; however, the ratio for commercial purposes is approximately four rubles per dollar. This is partially verified by comparing the airline fares from Western Europe to Moscow with the airline fare from Moscow to the same point in Western Europe. We found that the 10:1 rate is more accurate in terms of purchasing power; at this rate hotel rooms and restaurant meals are slightly less expensive by our standards, but most hard goods are somewhat more expensive.

-column card indicating the condition under which it d stopped. The machine could also simulate "race" nditions in relay circuits by inserting time delay de- ces of fixed values. This device used relays which had ree coils and fifteen contacts, five of which are transfer ntacts. A new version of this machine will permit in- uding time delays which will be variable by six incre- ents. This new design will also permit interconnecting her devices into the test circuits as well as including a inter and other devices to permit analysis of larger quential circuits.

6) A synthesis machine. This machine is intended to nthesize a relay circuit which in some sense is a best e for carrying out a particular switching function. avrilov felt that the algorithms for synthesis are not complete or as well known as he would like. How- er, he has developed his own theory of synthesis us- g simple bridge circuits, and can achieve minimal rms. A paper on this subject is expected to appear on.[11]

7) The error-correction machine. This development achine is intended to correct errors at the receiving d of a remote control circuit. It is to correct single er- rs, to detect double errors, and to be expandable for ultiple error correction and detection. The technique not that of Hamming, but one which they had devised. he message of N bits is considered as a mathematical oup and, therefore, the check bits are not necessarily stinguished from the data bits. This seems to imply at some form of dictionary look-up or word transla- on must be accomplished if the original data is to be constructed from this message. The information the- y measure of the number of bits being transmitted is pt being used; two representative bits out of four will cur if single and double error correction is done, but ur representative bits out of four will occur if single ror correction only is done.[12]

8) Remote control device. This is a switching device hich has been developed for remote control applica- ons. It utilizes square loop ferrite cores, power tran- stors, and relays to create a 52-bit switch. It can be sed to send several signals along a single twisted pair ne for approximately 30 to 40 kilometers without mplification. If some degradation is permitted it can be sed for about 200 kilometers. The frequency of opera- on was not specified, but it is inferred to be of the rder of a few kilocycles. This device returns an echo gnal to the sending station to verify the correct trans- ission of the switching instruction. It apparently uses me-division coding, with synchronization either by eans of special clock pulses or the alternating current ower frequency.

The analog computing equipment at this laboratory ad been built in 1957 or 1958. This Institute is also do- ing simulation in which a person is included in the loop. Such simulations are being used for purposes of design, testing of equipment, training, and predicting performance of complicated systems of equipment and people. Since the operational amplifiers available had responses as high as 30 kilocycles, problems were being solved in terms of seconds per run; occasionally problem solutions were as high as 15 runs per second.

The All-Union Institute of Scientific Information[13] (*VINITI*) (Fig. 8)

Fig. 8—All Union Institute of Scientific Information (VINITI).

Fig. 9—Professor A. I. Mikhailov.

The Director of this Institute is Professor Mikhailov (Fig. 9). The Institute is seven years old, and its purpose is to centralize collection and dissemination of scientific information from the USSR and the rest of the world. It is responsible for receiving foreign periodicals and for translating and disseminating these within the Soviet Union. It is also responsible for producing abstracts in many areas of science. Consequently, this Institute is deeply concerned with the field of information retrieval and it feels that its largest problem is the mechanization of its processes. As journals are received at the Institute, editors mark the parts of the article which are to be abstracted. The editorial board then

[11] *Automatika Telemechanika*. See also *Proc. Symp. on Switching heory*, Harvard University, Cambridge, Mass.; April, 1957.

[12] See M. V. Gavrilov, V. M. Ostinau, V. N. Rodin, and B. L. imofeyev, "Realization of schemes for discrete correctors," *Electro echnika, Doklady*, Academy of Sciences, USSR, vol. 123, no. 6; 1958.

[13] See: A. Kent and I. S. Iberall, "Soviet documentation," *American Documentation*, vol. 10, pp. 1–20 (see especially pp. 5 ff.); January, 1959.

sends this material to an appropriate individual somewhere in the Soviet Union for abstracting. After the material is returned to the Institute, the abstracts are edited and published. The individuals who do the actual abstracting are workers in the particular field and are paid for their contribution. Mikhailov found that it was necessary to have a computing center just to calculate what each abstractor should be paid. In the field of chemistry they have approximately 20,000 abstractors working all over the country, and they publish approximately 500,000 abstracts per year. This publication now appears as 24 volumes per year, and the lead time for producing an abstract is from two to four months after the appearance of the journal. Mikhailov estimated that the lag in the publication of a journal is itself from three to six months, and he hoped, by mechanizing his process completely, to reduce the total time from first typing of the original manuscript to the appearance of the abstract, to three and one-half months. One technique suggested by Mikhailov is to have the original typist prepare some sort of tape from which the final typesetting can be done.

On one wall of Mikhailov's office was a map of the world. From each country a string led to Moscow and an attached number indicated the number of journals received from that country. A few such figures are as follows:

United States	1416
England	844
France	491
Italy	368
Japan	304
Australia	143
India	142
Sweden	133
Canada	123
Germany	123
Netherlands	123
China	104
Spain	91
Denmark	71
Portugal	47
Argentina	42
Brazil	38
Chili	8
Iceland	3
Mozambique	3
Hawaii	2

The additional work on information retrieval and mechanization which this Institute is sponsoring in the Laboratory for Electro-modeling under Professor L. I. Gutenmakher will be discussed later as a separate topic.

Leningrad University imeni A. A. Zhdanov, Department of Mathematics

The building of the Institute of Mathematics and Mechanics of Leningrad University is a very old one, and was at one time a girls' school (Fig. 10). The exterior is an off-shade of yellow which is a very common exterior finish in Russia. The interior floors are parquet, but the wood is very rough and surprisingly of random width; it has been stained a dark red. In the Director's office were pictures of Khrushchev, Lenin, and Engel.

Fig. 10—Institute of Mathematics and Mechanics, University of Leningrad.

The appointments in the room reminded us of the earl 20th century in the United States.

At present the enrollment is 9000 day students an 6000 evening students. There are approximately 20 students in the Department of Mathematics, of whic 25 are at graduate level. The Department of Math matics includes four sections: Mathematics, Computin Mathematics, the Computing Center, and Astronom The department is divided into fourteen Chairs as fo lows:

Mathematical Analysis;
Ordinary Differential Equations;
Geometry;
Algebra and the Theory of Numbers;
Theory of Probability including Statistics, In formation Theory and Game Theory;
Mathematical Physics;
Computing Mathematics;
Fluid Mechanics;
Hydrodynamics;
Elasticity and Plasticity;
Theoretical Mechanics;
Mechanics of Rigid Bodies:
Celestial Mechanics,
Astrophysical Mechanics,
Stellar Mechanics;
Geodesy and Gravity.

In addition, the Mathematics Department has a gen eral service function to teach mathematical topics t other departments of the University. Except for one o two theses, the Mathematics Department is not yet per forming any experimental work in computing machines but they hope to inaugurate work in this field soon.

The Computing Center

This Computing Center has just recently beer founded and regards its first responsibility as training o students. Its second responsibility is service calculatin for the university, while last is calculating for outsid people. The Center has a URAL-I machine, variou punched card calculating machines, and several analo devices. One of these is the MPT-9 which contained 5

rational amplifiers; another is MN-M which is a desk machine capable of integrating a 16th-order equation. The amplifiers in these devices had drifts of the order of 10–15 mv over 15–20 seconds. The over-all accuracy of solution was of the order of 6 to 8 per cent. The Center expects to receive an ARAGATS machine within the coming year, and they plan to begin programming for this machine in the fall of 1959. They intend to install it on a lower floor than the present equipment, which suggests that the URAL-I machine will continue to be operated.

Professor Ladyzhenskaya has developed a scheme of solving a differential equation which utilizes large increments of the variables, but still provides very small errors. The Center has also written a translation routine which will modify the routines written for the Moscow URAL-I machine into routines for the Leningrad URAL-I. They recognize the desirability of having a uniform operating system for any given machine type, but at the moment they expect to develop their own algebraic programming system. A special machine for performing Fourier analysis was mentioned, but not seen. There was also an implication that a special machine was available for analytically manipulating formulas; it was also suggested that formula manipulation had been done on one of the known machines.

There is a branch of the Steklov Institute of Mathematics at the University of Leningrad under Professor S. I. Petrashen but the delegation did not visit it.

The Computing Center of the Ukrainian Academy of Science, Kiev

This Center grew out of a group headed by Lebedev in Kiev some ten years ago (Fig. 11). At that time Lebedev conceived and built the MESM machine, which was said to be the first sequence controlled computer in continental Europe. This machine still exists but it is used only for training purposes at another location. Following Lebedev's transfer to Moscow, the Kiev group continued to exist as an arm of the Institute for Precise Mechanics. In 1956 the group became a Computing Center in its own right; it was decided the group should build at least one machine for experience. The Computing Center's new 4-story building is slightly over one year old.

The Center, under the direction of Dr. V. M. Glukov, has designed and built the KIEV and the SESM computers. They have also designed and built specialized analog devices for performing analysis of rigid structures, as well as a 48-integrator electronic analog computer. The Center at Kiev is working on algebraic symbol manipulation and has just begun work on numerical analysis.

In addition to the previously mentioned machines, they also have a URAL-I. There is an active group planning the modernization and improvement of the KIEV. They are also actively working on the problem of character and pattern recognition.

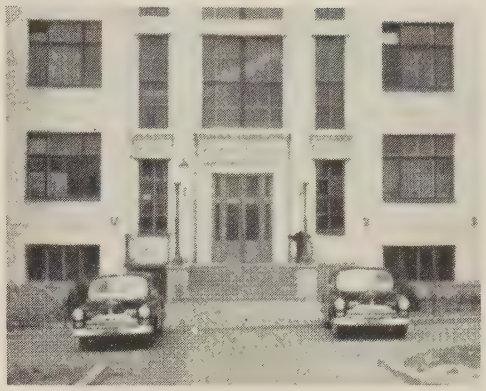


Fig. 11—Kiev Computing Center of the Ukrainian Academy of Sciences.

The Penza Computing Machine Factory

Penza is a town with a population of approximately 250,000 located 350 miles east and slightly south of Moscow. It is in an agricultural region and is surrounded by many smaller satellite towns. The region produces onions as a major agricultural product, and such manufactured items as textiles, compressors, bicycles, watches and computers. The industrial capacity of this town has developed since the revolution. Schools in the region include a polytechnic institute, a pedagogical institute, a civil engineering institute, and an agricultural institute. For university training, students must go to Kazan, Gorki, Moscow, Seratov, or Voronezh. The factory visited by the delegation also produces, in addition to digital computers, electronic test equipment, card punches and card reading devices, and some analog computers. It is part of a larger complex which produces watches and heavy equipment. Engineering personnel for the factory is obtained by sending manpower requirements to the Central Council on Production. A representative of the factory then participates in the selection of new employees through student interviews. This plant representative also obtains additional information on the student from the graduating commission at his school. When the engineer arrives at the plant he may, if he wishes, take evening courses in the polytechnic institute at Penza.

Plant managers come from technical backgrounds and do not receive specific administrative training; a plant manager, however, may correspond more nearly to a "director of engineering" than to a chief administrative officer.

The factory is in the process of planning a new plant which is to be constructed on the same 180-acre site during the next 7-year plan (1959–1965). At present the factory has about 4000 workers and has approximately two million rubles per year to provide rest homes[14] for about 800 people. Last year 6500 square meters of housing were added which provided 1-, 2-, and 3-room apartments for approximately 200 families.

[14] This term does not have the usual meaning. It means "vacation homes" or, more generally, "vacation opportunities."

At this factory we saw production of the URAL-I, and also the prototype model of the URAL-II. The characteristics and details of these two machines are included in another section of this report; only information about production techniques will be included here.

The assembly area looked quite modern, and had fluorescent lights. The windows were curtained and the walls painted a restful light blue color. Workers on the pluggable unit assembly line are paid on a piece-work basis and a punched card computing installation is used to calculate the payroll. Separate forms are used to record information about each worker's daily production.

The URAL-I is manufactured in modular fashion. Five basic modules approximately 8 feet×3 feet×14 inches are needed for the complete computer. Above the level of the console there are glass windows, and below it, metal doors. Cabling is done on layout boards as in this country. Capacitors, resistors, and some of the plastic parts of the machine are not produced at this plant, but most other parts are, such as ferrite cores and magnetic drums. Yield on core production is currently 50 per cent. There were 24 machines on the floor at the time. With a production rate of one every four days, more than 120 have been produced at this plant. There were no serial numbers on the machines which we saw.

Marginal checking equipment is brought to the machine while it is still on the production line, and the machine is checked out. A machine is transported as modules to the customer, who is responsible for connecting them together himself. Intermodule power connections are plugged but signal connections must be resoldered. It takes approximately two to three weeks after delivery for the URAL-I to be in operation at the customer's site.

The machine is built of ten types of pluggable packages. Test equipment capable of checking all types was available and provided both maximum and minimum marginal voltages for the package. The debugging crews had available a certain amount of special test equipment, such as a punched paper tape reader which could be used to read a test program into an almost operative URAL-I for its final checkout. Other devices included a paper tape verifier and a keyboard device similar to a desk calculator. The latter had 100 keys arranged in a 10×10 array and a plus and minus key. Apparently it permitted establishing a number of ten decimal digits for some particular test purpose. Special test equipment is also available for cycling the ferrite store through special test patterns and displaying the response as a geometric image on an oscilloscope. The usual complement of oscilloscopes and volt-ohm-milliammeters was also available.

The back panel wiring of the URAL-I was done on a systematic basis. There is a network of horizontal and vertical interconnections and power distribution wires which form a checkerboard pattern, each square of which is approximately three inches on the side. Withi each square are three different connectors associate with that square. Signal and power connections ar then made between the connectors and the checkerboar wire. In order to reduce the number of different types c packages in the machine, components are occasionall mounted on the base of the plugs. We were told tha these plugs, which use phosphor bronze springs, ha proved to be completely adequate. This checkerboar wiring occupies the top half of each cabinet module the bottom is reserved for power supplies which us selenium rectifiers. Signals between cabinets are brough out to lugs on the side faces of the cabinet which mat with similar lugs in the adjoining modules. Clockin pulses are distributed across each cabinet by heav buses. Both wiring tables and scale drawings are use to indicate where back panel connections are to be mad and components located. Plugs of solder are used be cause either rosin core solder is not available, or it i thought to be inadequate. No composition carbon re sistors were seen, either at Penza or elsewhere in Russia Low wattage resistors are deposited carbon, whereas higher power resistors are wire-wound units encased i ceramic. The capacitors physically resemble resistors Curiously, copper oxide rectifiers were observed in th back panel wiring. It was explained that these were needed in some cases to yield a sufficiently low for ward resistance combined with a reasonably high bacl resistance.

In manufacturing magnetic drums the drum itself i first machined to close tolerance and is then sprayed with the brown magnetic dispersion. Following this a lacquer coating is sprayed on the surface for protection Three clock tracks are physically engraved on one end of the drum. One of these establishes the origin reference of the drum, a second marks the beginning of each word and the third marks the position of each bit within a word. Recording density is 100 pulses per inch, and four positions are allowed between words to accommodate timing inaccuracies in the machine.

Three sets of heads are mounted on a drum. One set reads all the even tracks, while the second set reads the odd tracks. The third set is an erase stack for all tracks. Before permitting the drum to rotate, the structure which holds the head is heated for several minutes as a precaution against head scraping.

The price of the URAL-I was quoted at 1.1 million rubles, but as soon as the URAL-II is in production, this price will be halved.

Using the same basic components as the URAL-I, the product engineering group at Penza has designed the URAL-II, in which a different internal organization is used to achieve a much higher speed. The URAL-II was said to be fifty times as fast as URAL-I, but 100 times more effective because of improved organization. It will sell for 1.5 million rubles and its details are given

sewhere in the report. We saw what appeared to be a ototype model. It was being debugged prior to production and apparently routines were being prepared for it. t present there are more customers than machines, d the factory does not have to maintain a sales force. ney do, however, have people who write equipment scriptions and send them to potential users. Occaonally factory representatives even visit these potenal users to explain the usefulness and desirability of e digital computers.

In another building we were shown about 40 card unches. About half of these were 90-column machines d the other half 80-column machines; all were genally similar to United States designs. These units apeared to represent the most recent design in Soviet unched card equipment. We saw also a 500 card per inute sorter which closely resembled a corresponding merican product. It had electro-mechanical sensing the holes and a set of switches for suppressing specific w selections as in American sorters. It also had a spe-al attachment which permitted collating on 12 colmns by means of a plugboard and 12 auxiliary brushes.

Specific Machines

The Soviet development of internally sequenced comuters began with the MESM machine, conceived and onstructed by Lebedev at Kiev. The development the field, so far as the Academy of Sciences is conerned, centered around Academician Lebedev and is Institute for Precise Mechanics and Computing echniques. There also has been some parallel developent by other laboratories or institutes which are conected with other ministries of the Soviet government r industrial organizations. At the present time cooperaon between the Academy's Institute and industrial lants is beginning, and future machine development n Russia may well turn out to be a cooperative venture.

In comparing Russian machines with United States achines, it must be noted that Soviet designers place onsiderable emphasis on analyzing the set of problems o be encountered by a given machine. A fairly detailed tudy is made of the number of each kind of instruction hich occurs in some class of problems, and on the basis f this statistical distribution, the speed of the machine quoted as so many operations per second. Unforunately there are several sets of statistics in use; and rom our information, it is not always clear as to which et applies to a particular machine. Further, there is lso some disparity between the statistics reported at arious locations. In the following discussion and in able I, pp. 86–87, the statistical weighting has been sed which is believed to be correct for each machine.

For some machines it is uncertain as to which might e the correct basis; the speed of the machine in operaons per second is not likely to change radically from ne statistical basis to another.

The so-called BESM-II statistics as reported at Moscow are:

30 per cent add-subtract,
30 per cent multiply,
3 per cent divide,
37 per cent all other operations.

The so-called STRELA statistics as reported at Moscow are:

25 per cent add-subtract,
30 per cent multiply,
2 per cent divide,
10 per cent address modification,
33 per cent all other operations.

The URAL-I statistics as quoted at the Penza factory are:

17 per cent add-subtract,
17 per cent multiply,
3 per cent divide,
33 per cent transfer,
30 per cent all other operations.

The figures quoted to us by the Leningrad group differed rather significantly. According to them the BESM-II statistics are: 68 per cent add-subtract and 32 per cent multiply, while the STRELA statistics are 75 per cent add-subtract and 25 per cent multiply. It is believed that the statistics quoted to us in Moscow are more likely to be correct.

Table I summarizes the information received on all digital computing machines which were seen. In order to make this table complete, a small amount of information has been carried forward from the Scott, Carr, Perlis, Robertson report.[1] Where there is considerable uncertainty as to the accuracy of a figure, it is followed by a question mark.

BESM-I[15]

This machine was originally constructed in the early 1950's with an acoustic delay line store (Fig. 12). This store was later changed to a Williams type electrostatic store and recently was again changed to a magnetic core store of 1023 words of 40 bits.[16]

The core storage element of BESM-I was designed approximately four years ago and it is clearly an early model of such a store (Fig. 13). The store is expandable to 2047 words, although there was no indication that this expansion would be done. It was indicated that only one BESM-I machine has ever been built in the Soviet Union. The machine requires seven dc voltages between +400 and −400, and is physically constructed of fairly large pluggable units, using vacuum tubes of the general dimensions of the 6SN7. The tape transports connected to this machine are modified audio transports. There are only two tracks, one for information and one for

[15] S. A. Lebedev, "High speed electronic calculating machine of the Academy of Sciences of the USSR," *J. Assoc. for Comp. Mach.*, vol. 3, p. 129; July, 1956.

[16] It will be noticed that the size of many stores in Russian machines is (2^n-1) words in size. This is because storage location zero is permanently reserved as the location for the numeric constant zero.

TABLE I

Soviet Computing Machines

Machine	Operational Date	Arithmetic Characteristics								Control Characteristics			Storage								
													Core Storage		Magnetic Drum			Magnetic Tape			Read Only	
		Addition Time[2]	Multiplication Time[2]	Division Time[2]	Average Speed[1] (operations per second)	Word Length	Number Representation	Number Range	Serial/ Parallel	Fixed/ Floating Point	Instruction Format	Number of Instructions	Clock Rate (Kcs.)	Size (Words)	Cycle Time (Microseconds)	Number of Units	Words per Unit	Transfer Rate (Words per second)	Number of Units	Words per Unit	Transfer Rate (Words per second)	Size (Words)	Cycle Time (Microseconds)
STRELA	1953	—	500(?) μs	—	2000	43	Binary	—	Parallel(?)	Floating	3 address 1 per word	—	—	None—Barrier Grid Electrostatic Store —1023 words		—	—	—	1[6]	200,000	1000	Yes	
BESM-I	1953	—	270 μs	—	7–8000	39; Mantissa: 32+sign; Exponent: 5+sign	Binary	—	Parallel	Floating	3 address 1 per word	31	—	1023	10	1	5120	—	4	30,000	—	400	—
URAL-I	Approx. 1953 (design) 1955 (production)	10 ms	10 ms	20 ms	100	36	Binary	±1	Serial	Fixed	Single address 2 per word	29	7	None	None	1	1024	100	1	40,000	75	None	
BESM-II	1959 (prototype)	70 μs	230 μs	230 μs	8–10,000	39; Mantissa: 32+sign; Exponent: 5+sign	Binary	—	Parallel	Floating	3 address 1 per word	31(?)	—	2047	6	Up to 3 (2 installed now)	6000	12,000	4	30,000	400	None	
URAL-II	1959 (prototype)	—	—	—	5000	40; Mantissa: 32+sign; Exponent: 6+sign	Binary	$\pm 1\times 10^{\pm 19}$	Parallel	Both	Single address 2 per word	40	200	2048	12	Up to 8	8192	5000	Up to 10	700,000	1000	None	
SETUN	1959	180 μs	360 μs	(none)	4000	18	Ternary	±9	Serial	Fixed	Single address 2 per word	27	200	81	—	1	2268	2000		To be added		—	—
KIEV	Probably 1960	—	200 μs	—	5–6000	41 (?)	Binary	±1 (?)	Parallel	Fixed	3 address 1 per word	—	asynchronous	1024	10	Up to 3 (1 installed now)	8192	5000	—	None	—	512	3
M-20	1959	—	—	—	20,000	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
ARAGATS	Probably 1960	—	—	—	15,000	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Typical large U. S. scientific machines[4]	Early 1959	—	—		5–7000 for production machines; up to 15,000 for one-of-a-kind[3]	36–40	Binary, Binary-coded decimal	Fractional or Integer	Parallel or Mixed	Both	1, 2, or 3 address 1 or 2 per word	Up to 200	500–2000	4096–32,768	6–12	2–4	4096–50,000	10,000–50,000	Up to 20[5]	Up to 1,000,000	2500–10,000	None	
Typical large U. S. scientific machines[4]	Early 1960	—	—		20–25,000 for production machines[3]	36–48	Binary, Binary-coded decimal	Fractional or Integer	Parallel or Mixed	Both	1, 2, or 3 address 1 or 2 per word	Up to 200	500–2000	4096–32,768	2–12	2–4	4096–50,000	10,000–50,000	Up to 20[5]	Up to 1,000,000	2500–10,000	None	

[1] These speeds are quoted with respect to some statistical distribution of instruction types. The particular distribution which is appropriate is not always known. These rates are, as appropriate, three address to single address, fixed point to floating point operations per second.

[2] These speeds usually include necessary accesses to the store, including that for the instruction fetch.

[3] In arriving at these figures, the BESM statistics were used and a factor of 2.5 was used to adjust the single address machines to a 3-address basis; floating-point execution times were used. These rates are therefore 3-address floating point operations per second. Admittedly, this measure does not allow for sophisticated instruction types (*e.g.*, indexing, buffered input-output) but it does measure the ability of a technology to produce switching circuits in a given speed range.

[4] Does not include LARC, STRETCH or machines which are intended primarily for data processing; *e.g.*, 501, 7070.

[5] May be much larger in special cases, as in some data processing applications.

[6] Only one tape unit was seen on the STRELA at the Academy of Sciences Computing Center: four tape units have been reported on other STRELA's.

TABLE I (*Continued*)

Machine	Number Form	Number of Input Devices	Number of Output Devices	Input-Output								Power (Kva)	Number Components	Price (Rubles)	Quantity Produced	Designer or Principal Personnel
				Perforated Tape			Card Reader Rate (Cards per Minute)	Card Punch Rate (Cards per Minute)	Printer							
				Width and Kind	Size (Words)	Transfer Rate (Words per Second)			Columns	Number Characters	Speed (lines per minute)					
STRELA	—	1–5 card readers	1–2 card punches	—	—	—	60	60	10	Numeric	900–3000	147	7000 tubes 50–60,000 diodes	—	Estimated 10–15	Brusenzov Basilevskiy
BESM-I	Binary(?)	1–paper tape reader	1–paper tape punch	Paper	—	20	None		14	Numeric	900	75	4000 tubes	—	1(?)	Lebedev
URAL-I	9 Decimals and sign	1–Perforated film	1–Magnetic Tape 1–Printer	Film 35 mm.	10,000	75	None		19	Numeric	100	8	800 tubes 3000 diodes	1 million	>120	Basilevskiy Rameyev
BESM-II		Probably paper tape reader	Probably paper tape punch 1-Printer	—	—	—	Probably None		14	Numeric	900	—	—	—	To be produced	Lebedev
URAL-II	8 Decimal Mantissa+sign and 1½ decimal Exponent+sign	1–12; with special decoder: up to 100	1–card punch and 1–printer minimum; with special decoder: up to 100	Film 35 mm.	10,000	150	300	100	16 or 96	Numeric	1200	25	—	1.5 million	To be produced	Rameyev
SETUN	—	Photo-cell paper tape reader	1–paper tape punch 1–printer	German teletype equipment	—	400 chars per second	None		German RFT Teleprinter			—	4000 cores, 40 tubes, 4000 diodes, 100 transistors	—	1	Brusenzov
KIEV	—	1–Perforated film now	1–Printer now	Film 35 mm.	10,000	75	—	—	19	Numeric	100	—	2000 tubes	—	1	Glushkov Dashevskiy
M-20	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
ARAGATS	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Typical large U. S. scientific machines[4]	—	Usually card reader, magnetic tape, or paper tape	Usually card punch, printer, magnetic tape	Paper, teletype	—	1000 chars per second	250	120	120	Alpha-numeric up to 1200 (numeric only up to 1800)		Up to 100	3–5000 tubes 15–20,000 diodes	>$1 million	Hundreds	Various
Typical large U. S. scientific machines[4]	—	Usually card reader, magnetic tape, or paper tape	Usually card punch, printer, magnetic tape	Paper, teletype	—	1000 chars per second	Up to 2000	Up to 250	120	Alpha-numeric up to 1200 (numeric only up to 1800)		Up to 100	All transistor and diode	>$1 million	—	Various

Fig. 12—Console and general view of the BESM-I.

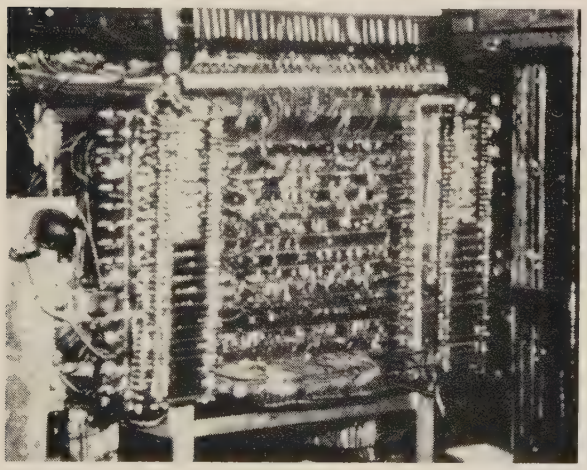


Fig. 13—Magnetic core store of the BESM-I.

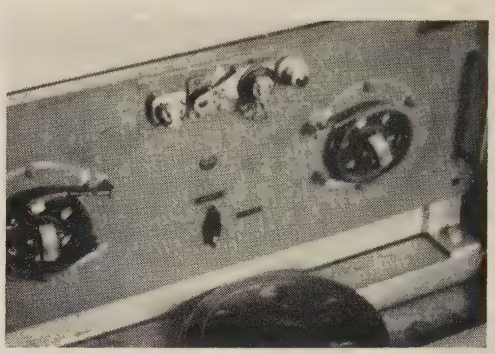


Fig. 14—Magnetic tape unit of the BESM-I.

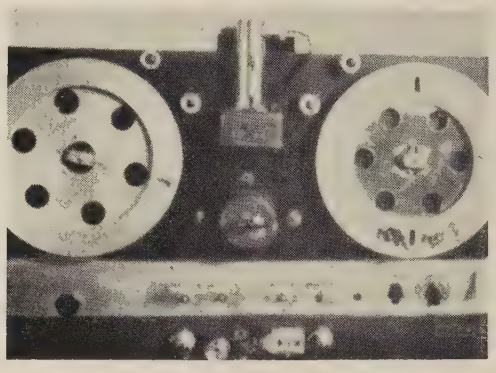


Fig. 15—Paper tape reader of the BESM-I.

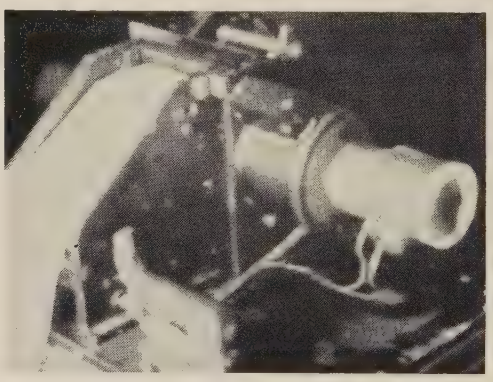


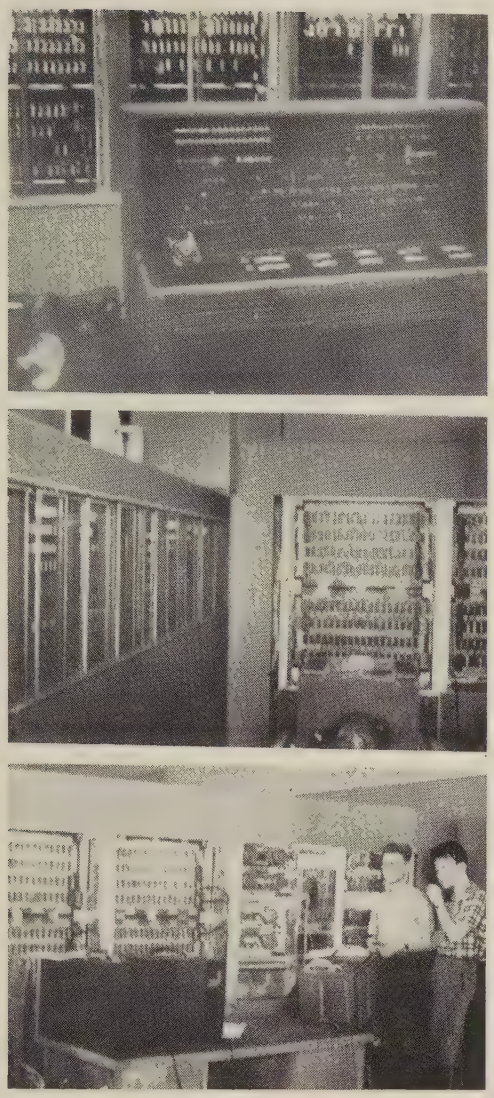
Fig. 16—Output printer of the BESM-I.

timing signals (Fig. 14). The machine was reported to be asynchronous; however, after detailed inquiry it developed that it had an internal clock. Its operations could be variable in time of execution, but only by increments of the clock interval.

The input device to the BESM-I is a photocell paper tape reader (Fig. 15). The output includes a high-speed, 14-column, 15-lines per second numeric printer, producing only one copy (Fig. 16).

The BESM-I has a supplementary 400-word, changeable, read-only store of the diode function table type. There are several locations at which pluggable panels can be manually changed in order to provide certain standard subroutines to the machine without repeated reference to the main core store.

The mean free time between failures on the BESM-I was reported to be approximately 6 to 8 hours; about 70 per cent of the breakdown is in the input-output devices and other electro-mechanical equipment. The BESM-I is operated by the programmers who use it, and therefore in the machine records no accounting is made for restarts or reruns which are due to machine failures. Good performance statistics were not available, but the maintenance engineers (one man per shift) thought there was about 8 per cent lost time. Associated with the BESM-I is an off-line printer which is connected by teletype with the Academy Computing Center. This is probably a convenient method for transmitting problems to BESM-I from the Computing Center, which still regards BESM-I as one of its operating machines.



ig. 17—The BESM-II. (*Top*) console; (*center*) *left*, arithmetic section, *right*, drum section; (*bottom*) drum and tape section.

The general appearance and marginal workmanship isible on BESM-I certainly marks it as an older, often-nanged machine.

ESM-II

This machine is organizationally like the BESM-I nd presumably will accept routines which were written or BESM-I (Fig. 17). Its construction and circuit tech-ology are different, however. Physically, it consists of 4 cabinets, each about 3 feet wide and about 7 feet igh; this includes the cabinets for the four tape units. ts internal store is initially 2047 words but will be ex-anded at a later date to 4095; it is a word-organized nd-fire design (Fig. 18). The cores themselves are 1.4 m outside diameter and each plane is 128×48. There re 16 such planes in the store. The store is designed ith 48 bits per word, although only 40 of these are re-uired by the machine. The cycle time of the store is 6 sec, although the basic cycle time of the machine is 10 sec; this is a carry-over from the design of BESM-I here 10 μsec were required for a cycle of the electro-

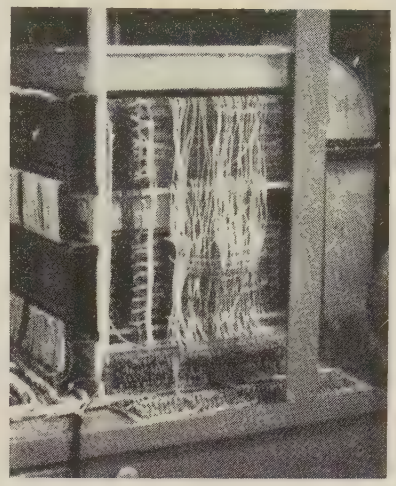


Fig. 18—Magnetic core store of the BESM-II.

static store. Of the 6-μsec store cycle, 1.5 μsec are required for address decoding, then 0.6 μsec for reading.

Two cores are used for each bit. There were three arguments advanced to us for this choice. One was that uniformity of cores was sufficiently bad that only by using two cores per bit could a yield as high as 80 per cent be achieved from the core production. The second possibility is that by using two cores per bit the load which the switch core in the end-fire switch must drive is constant. The third possibility suggested to us was that the second core on each bit provided redundancy in case the first one fractured or failed. The current to drive the switch cores is obtained from large vacuum tubes and, as in the United States design, the core stack is force air-cooled. In order to avoid extraneous ground noises twisted pair buses have been used.

Between stages of the shift register is a 0.3-μsec delay line; even so, to shift any number of places less than 16 will require 65 μsec because of some peculiarity of the internal structure. Addition time is 70 μsec, including four accesses to the store; multiplication and division are each 230 μsec, including accesses to the store. The word format is 32 bits plus sign for the mantissa, and 5 bits plus sign for the characteristic.[17]

There are two magnetic drums of 6000 words each (Fig. 19) and four magnetic tapes of 30,000 words per tape (Fig. 20). As in BESM-I, the magnetic tapes have two tracks and move at 2 meters per second. One track is for information and the other for timing signals. Starting and stopping is done at the reel, which implies that these units are efficient only for transferring large blocks of information. 1.5 meters of tape is allowed between blocks of information and the designers felt that they could guarantee interchangeability of tape between transports. Tape density is 7 to 8 bits per millimeter, and the method of recording is discrete pulses on a saturation bias background. A modulo 32 count of the

[17] While this accounts for only 39 bits, the store was definitely reported as having a 40-bit length. There may be a parity check.

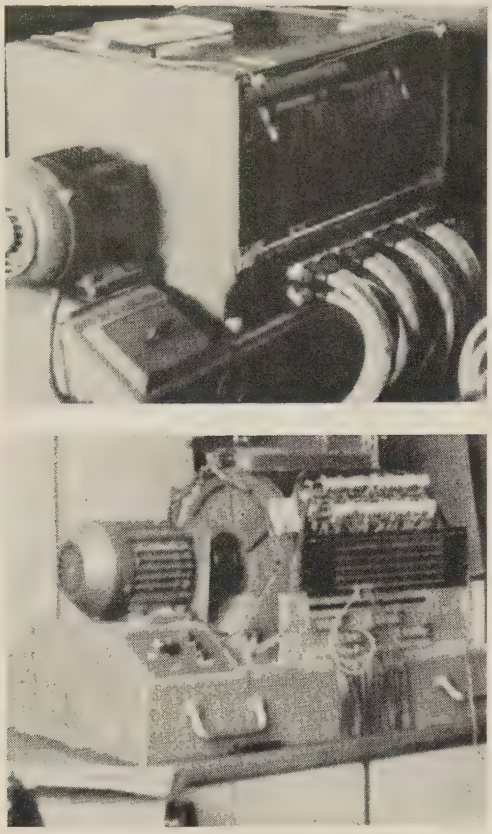


Fig. 19—(*Top*) magnetic drum on the BESM-II; (*bottom*) same drum on the KIEV.

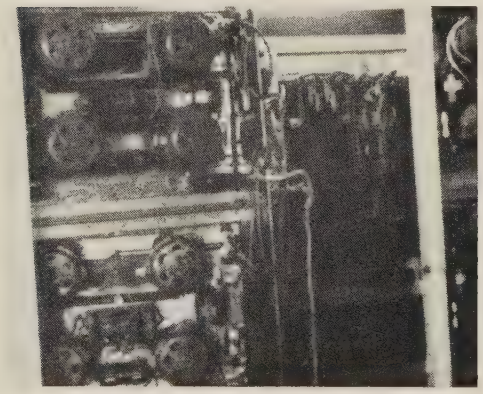


Fig. 20—Magnetic tape units of the BESM-II.

number of words transferred is automatically made for tape records and blocks of drum information. This count is stored in a special 5-bit counter which can be addressed by the routine and therefore used to verify that the correct number of words has been transferred.

Germanium diodes have replaced the vacuum tube diodes of BESM-I. The new style of pluggable unit construction does not use printed circuits in the model which we saw, but it is expected that printed boards will be used in the production model of this machine (Fig. 21). At the time we saw the machine it was in the final stages of debugging. We were told by Dorodnitsyn that it would be fully operational in June, 1959. Miscellaneous remarks led us to believe that some amount of production time has already been realized from this model, and that routines for it have probably already been checked out. The decision has been made to place this machine in serial production.[18] The location of production was unspecified, although it was thought that it would probably not be in Moscow or Penza, but might be in Siberia. The size of the BESM-II production was suggested to be a few tens of units.

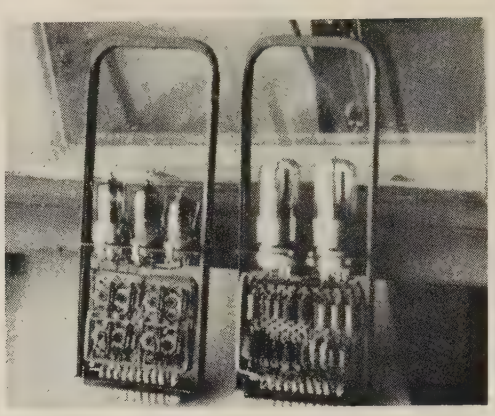


Fig. 21—Pluggable packages of the BESM-II.

There were three independent groups of engineers working on the BESM-II. One of these was from Lebedev's Institute which is responsible for completing and debugging the machine; a second group was from the Computing Center which will have to maintain it; and the third group was from the Georgian Academy of Sciences at Tbilisi, which apparently is scheduled either to get or to build a BESM-II.

In debugging this machine, test routines and marginal checking are being used. There is manual control permitting ± 10 per cent variation in all voltages. Design tolerances are ± 10 per cent on the 6-volt heaters, ± 4 per cent on the negative bias voltages, and ± 2 per cent on the positive supply voltages.

We were told that the design of the BESM-II had been completed in a few months and that the biggest job which faced the Institute was not that of completing the machine, nor of designing it, but rather the time of preparing production drawings for the factory.

The BESM-II is designed for a different final checkout procedure than is common in the United States. One complete machine is assembled at the factory and thoroughly checked out. Since each cabinet of the machine consists of several removable panels (Fig. 22), this completed and tested machine is then used as a test device in which production panels are tested in the environment of a completely checked-out system. Such a removable panel for BESM-II contains approximately 50 plug-in packages, and is removable as a unit by

[18] The Russians use the phrase "serial production" to indicate that an item is to be made in succession in a production facility. Our term of "mass production" is used to describe the scale of activity concerned, rather than the number of items produced; *e.g.*, production of one battleship would be regarded by them as mass production but not serial production.

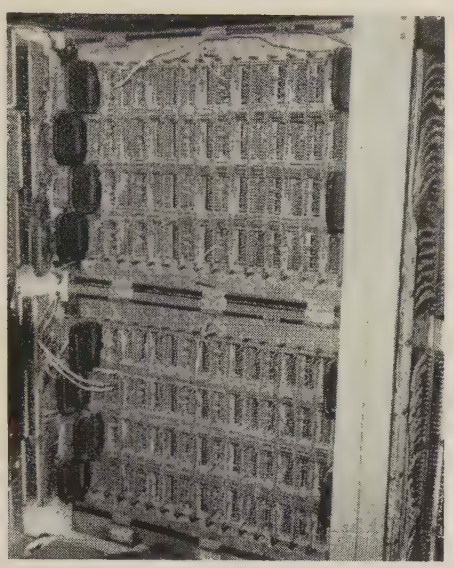


Fig. 22—Rear panel wiring of the BESM-II.

eans of screws. Most of the connections to such a anel are made by plugs, although some signal leads re soldered connections and sometimes also coaxial able. The intent is to produce the structural frames of ach machine, and to hand-inspect them. Panels will be ndividually tested at the factory in the environment f the previously checked-out and completed machine. new machine will be assembled for the first time on he customer's premises, and any remaining troubles ill have to be dealt with at that time.

BESM-II has punched paper tape input and output. With respect to the statistical weighting of 68 per cent dd-subtract, and 32 per cent multiply, the BESM-II perates at 10,000 floating-point 3-address operations er second.

URAL-I (Figs. 23–26)

A 19-column rotating wheel printer is in production or URAL-I. Its speed is 100 lines per minute and the printing mechanism includes a facility for suppressing printing in any desired column. The URAL-I magnetic ape contains six channels, three of which are used at a ime to read the 12 lines of information required for the 36-bit word. There are 104 words per meter which implies that the recording density is 1248 bits per meter. The linear tape speed is 0.75 meter per second resulting n a transfer rate of 75 words per second.

Characteristics of the URAL-I are summarized in Table I. Appendix I gives the instruction repertoire of his machine.

URAL-II

This machine has a 200-kc clock rate, compared with he 7-kc rate for URAL-I. In addition it is a floating-point, parallel machine, constructed of germanium diodes and vacuum tubes. It contains several new instructions, including those for floating-point. It contains er-

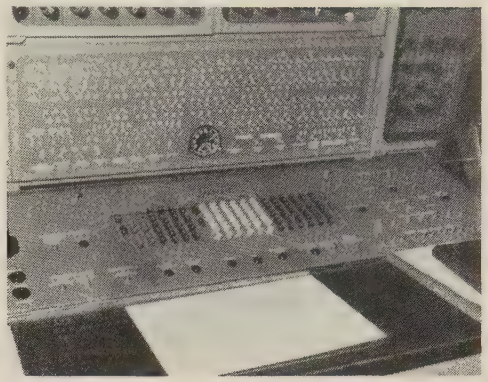


Fig. 23—Console of the URAL-I.

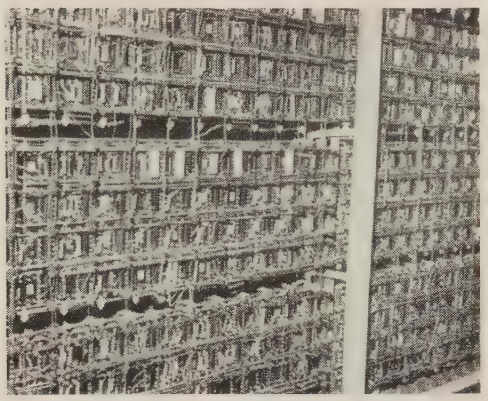


Fig. 24—Rear panel wiring of the URAL-I.

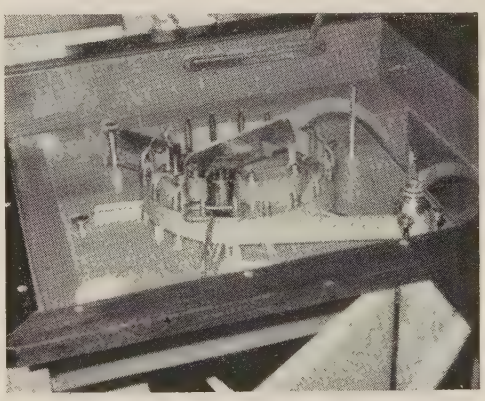


Fig. 25—Perforated film unit of the URAL-I

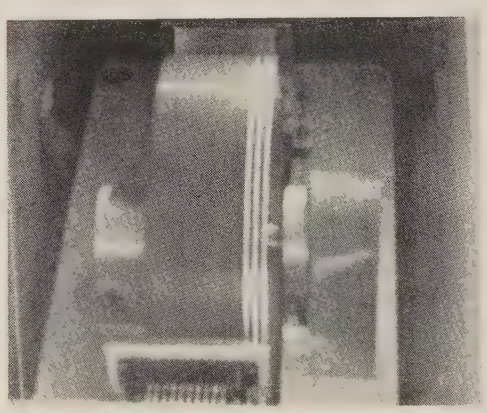


Fig. 26—Magnetic drum of the URAL-I.

ror-checking circuitry, including automatic computation of check sums for input-output devices. Other possible input devices mentioned were punched cards (300 per minute), communication lines, and random number generators. The usual output devices will be a printer and card punch (100 per minute). The printer is numeric only, 20 lines per second, and can be either 16 or 96 columns. Connection between the URAL-II and its input-output devices is through the arithmetic unit where a check sum is formed on every 100 words. A special selection word using a separate bit per input or output device allows up to 12 input devices and 12 output devices without the need for a decoder. Information can be transferred to several output devices simultaneously.

The storage hierarchy in URAL-II is a 2048-word core store (12-μsec cycle), an 8192-word drum (maximum of 8 drums), and magnetic tapes of 700,000 words each up to a total of 5 million words. Each of the 20 planes in the core store consists of four 16×16 arrays assembled on thin plastic frames (1/32 inch $\times$ 4 inches $\times$ 4 inches). The store operates in a coincident current mode, has only one core per bit, and has four sense windings. By selecting two Y wires and one X wire, two bits are read out from the 64×64 plane at a time. It therefore can be thought of as 4096 20-bit words, or 2048 40-bit words. They achieve a 50 per cent yield on cores made at the factory. Core windings are soldered to a mounting wire which is held to the frame by being threaded through a pair of holes. Special test equipment is available for cycling the store through special patterns. Drive current tolerance is ±30 per cent.

The punched tape input and output is similar to that of URAL-I. Continuous loops of perforated 35-mm movie film are read at the rate of 150 numbers per second (1.5 meters per second linear motion). The reading device uses photo diodes. The tape has eleven channels, and one word is written across it in parallel; decimal digits are written along the tape in 8-4-2-1 code. A special 9-column decimal keyboard is used for tape preparation. Normally a URAL-II has one punch station but two readers which operate in parallel to compare 200 numbers per minute.

The URAL-II magnetic tape is also similar to that of URAL-I. 35-mm film is used as a base for the magnetic medium, and punched holes mark the records. The tape reads 1000 words per second at a linear tape speed of 1.5 meters per second.

The word format is: 8 decimal digits plus sign for the mantissa (33 bits), and 6 bits plus sign for the exponent. The range is therefore $\pm1\times10^{\pm19}$ and the word length is 40 bits. Based on the statistical distribution of 17 per cent add-subtract, 3 per cent divide, 17 per cent multiply, 33 per cent transfer, and 30 per cent other operations, the speed of the URAL-II is 5000 operations per second.

The URAL-II instruction repertoire is given in Appendix II.

STRELA

This machine (Figs. 27–29) was designed by an industrial construction bureau and serially built at the Moscow Computing Machine plant; it is now referred to, because of its age, as the "Old Woman." It is a big machine and uses specially designed electrostatic tubes in the store. The cycle time of the barrier grid store is 500 μsec, and 27 points are regenerated between consultations. One STRELA had five card readers and two card punches while a second STRELA had only one of each. The machine at the Computing Center operates 7 days a week, and requires a maintenance staff of three engineers per shift. About 18 hours per day of useful running time can be achieved; 3 to 4 hours per day is devoted to preventive maintenance and the balance of the day is unscheduled maintenance. This machine was designed in 1948, although the installation at the Academy Computing Center was not made until 1957. The precise number of machines manufactured is uncertain but it was suggested that at most a few tens had been constructed.

The STRELA tape unit is approximately 4 inches wide (Fig. 30). A word is written in parallel across the tape which is recorded at a linear density of 2.5 bits per millimeter. The reading rate is 1000 numbers per second and reading is in terms of a block. For reliability great emphasis is placed on programmed check sums.

The STRELA, like the BESM-I, also has some interchangeable wired subroutines which can be used for such things as sine, logarithm, etc. It also has about ten groups of stored constants of 16 bits each. The card readers and card punches were quoted at about 60 cards per minute.

The inadequate reliability of the STRELA store leads users to program check sums into their problems. There is some possibility that a core store may be retrofitted to this machine.

SETUN

This base-3 machine being constructed at Moscow State University appeared to be in operation when we saw it (Figs. 31–33). It was explained that the choice of base-3 was made because it can be shown that in some sense a base of 3 provides the most efficient utilization of equipment.[19] Since a base-3 electronic technique is not available, they decided to construct a base-4 machine and to utilize only three of the four possible states. The unused fourth state in each case is available for some form of checking. This machine is regarded as experimental, and as an educational training program for engineers. In part they felt that SETUN was a protest against the huge, complicated machines being built elsewhere. It was thought easier to operate a simple ma-

[19] ERA Staff, "High-Speed Computing Devices," McGraw-Hill Book Co., Inc., New York, N. Y., p. 84; and Staff of Computation Laboratory, "Synthesis of electronic computing and control circuits," *Ann. Harvard Computation Lab.*, vol. 27, p. 145, 1951.

Fig. 27—General view of the STRELA.

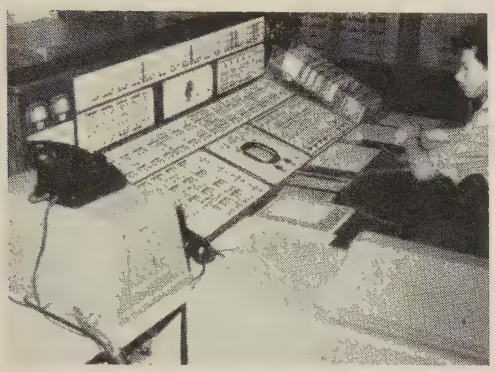


Fig. 28—Console of the STRELA.

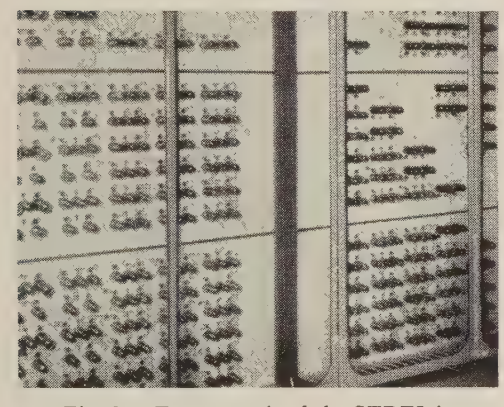


Fig. 29—Front panels of the STRELA.

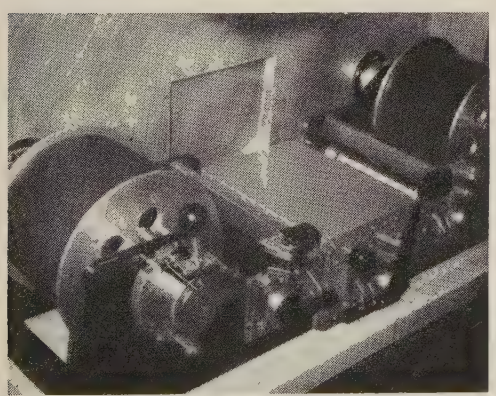


Fig. 30—Magnetic tape unit of the STRELA.

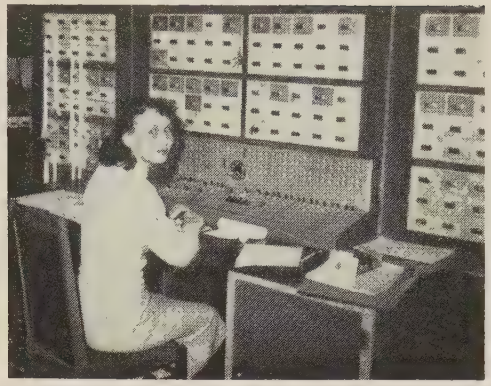


Fig. 31—Console and general view of the SETUN.

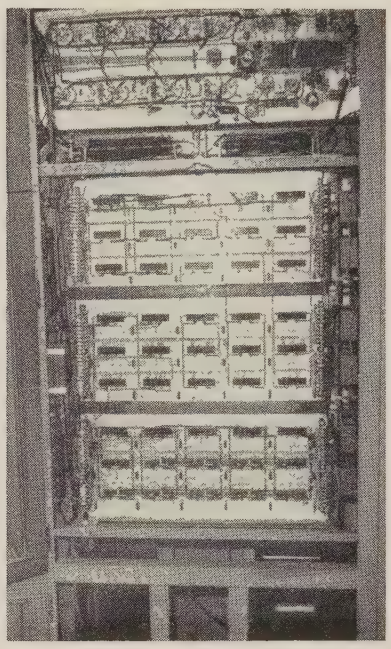


Fig. 32—Rear view of the SETUN.

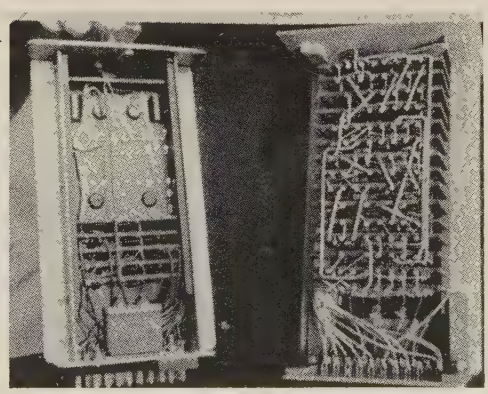


Fig. 33—Pluggable package of the SETUN.

chine at their center. The machine contains 4000 magnetic cores, 4000 germanium diodes, approximately 100 transistors, and 40 vacuum tubes. It operates at a 200-kc clock rate. It uses 1-mc transistors which are rated at 150 milliwatts dissipation at 25°C, but can tolerate a maximum of 100°C.

SETUN has only 81 words of storage and 27 different instructions. It is a single-address, fixed-point machine, with 18 ternary digits per word. The point is fixed between the second and third digits from the left. It is serial and contains two instructions per word. There is no divide instruction.

The ferrite core store can be regarded as having 162 9-digit words because the half words can be addressed. The drum store contains 2268 half words. Number representation of SETUN requires 2 binary digits per base-3 digit; therefore, a 9-digit, base-3 word will require 18 tracks on the drum. There are three such groups of 18 tracks on the drum, or a total of 54 heads. In each band of 18 tracks there are 756 words recorded in parallel; there are thus 756 bits around the 13-inch circumference. It is planned to add magnetic tapes to this machine at some later date.

Addition time is 180 μsec including all accesses. Fetching of the next instruction is overlapped with execution of the previous one. Multiplication time is 335 μsec and transfer of control is 100 μsec. SETUN includes a normalizing instruction (shifting operations to facilitate programming of floating-point), one index register, and teletype input and output. The German type RFT teleprinter is partially base-9 and partially base-3. A 9-digit word is printed as two base-9 digits, then one base-3 digit, then two more base-9 digits. The characters used are:

Base-9 ϟ,Ɛ,ƻ,ɪ,0,1,2,3,4,
Base-3 i,0,1.

Five-level punched paper tape is used for the input and output.

KIEV

This machine is expected to be completed by December, 1959; a substantial part is already operational (Fig. 34). It is in five cabinets in a semicircular arrangement, and requires a floor area of approximately 20×35 feet. It is truly asynchronous and operates at a speed of 5000 to 6000 operations per second. It uses static flip-flops but diode-transformer gates. Pulse sources are blocking oscillators having two independent transformers in the plate circuit. One is for the regeneration required by the blocking oscillator itself; the other, for driving the output. The machine has arithmetic, logical, and block-transfer instructions, is binary and has a word length of 40 bits. The arithmetic unit is capable of adding, shifting, multiplying, and dividing.

The principal store[20] is a 1024-word ferrite store of the end-fire BESM-II type. The store is autonomous ar has separate checking, which suggests that there ma be a wired-in independent test routine. There is also 512-word read-only store which is based on a tran former technique; its read time is approximately 3 μse This passive store, when expanded to larger size, w contain the automatic program and the binary-t decimal and decimal-to-binary conversion routine There are also eight words of storage which can be s from switches. There will be three drums of the san type as the BESM-II; only one is presently installe At the moment the input and output is paper tape.

There are seven types of standard circuits in th machine. Each cabinet of the machine contains its ow power supply. Because of this modular constructio and the truly asynchronous organization, it was o served that expansion and modernization is very simpl It was also stated that convenient marginal "conditio for prophylaxis" exist. An improved version of th KIEV machine was under way and we noticed a su stantial amount of BESM-II type equipment on han for this purpose. In the modernized version, arithmet operations might be automatically repeated und marginal conditions and the result compared; this is type of checking being considered.

SESM

This machine (Fig. 35) is a special-purpose digit computer which is intended to solve sets of linear equ tions of orders up to 120. The design is expandable orders of 480, and is based on the Gauss-Seidel iter tion technique. The solution time depends on the nun ber of zero elements in the matrix and on the distrib tion of these elements. For an 18×18 matrix which wa rather ill-conditioned, a solution had been achieved 148 iterations and about two hours. A rough rule thumb for the time in seconds required for one iter tion is: the number of nonzero elements divided by 20

The input is presently punched paper tape at a ra of 27 decimal digits per second; the speed at which th machine can achieve a solution is limited by this devic The output is on an adding machine type printer. Th SESM was conceived by Lebedev but designed and co structed by Rabinovich. A magnetic drum contains 3 bit recirculating registers for arithmetic purposes. Th recording density is three bits per millimeter. The i ternal clock rate is 50 kc.

Special-Purpose Analog Computer at Kiev

This machine was designed to analyze the stresses three-dimensional rigid structures (Fig. 36). It was co ceived and constructed by Professor Pukhov. It co sists of three panels, each of which has 48 potentiomete arranged in six rows and eight columns. These are us to represent the elastic constants of the bars. Up to

[20] This particular type of store is frequently referred to in Russia as the "Z" system.

[21] This rule-of-thumb doesn't agree with the previous example, b these were the data that were collected.

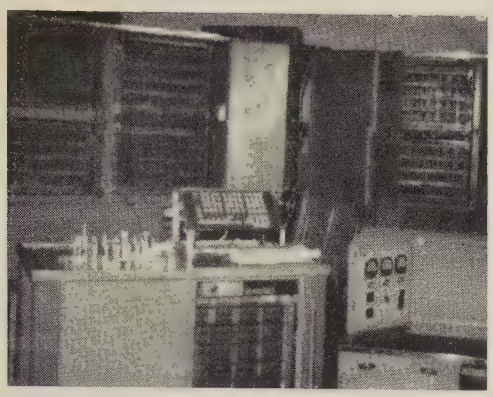


Fig. 34—General view of the KIEV.

Fig. 35—General view of the SESM.

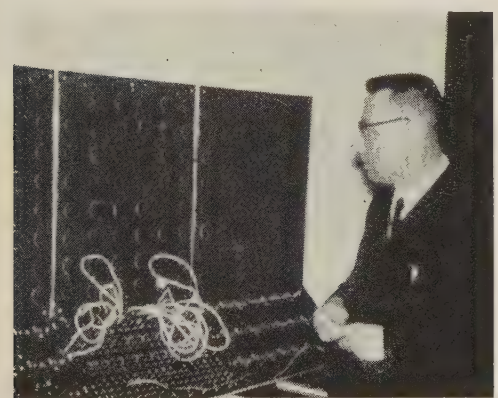


Fig. 36—G. E. Pukhov and the structure analyzer.

ible rods and 9 rods in torsion can be accommodated the model. This machine uses all passive elements, rates on dc, and achieves approximately 5 per cent uracy. It can also be used to give dynamic solutions, nough normally it is used for static solutions. It pro- es three-dimensional solutions, rather than the two- ensional ones obtained by other workers. They are nning a new desk-size machine of similar kind, ca- le of accommodating 70 rods.

-M and MPT-9 Analog Computers (Figs. 37 and 38)

These two machines are well known and have been ibited at various trade fairs and exhibitions. No new rmation about their capabilities was obtained.

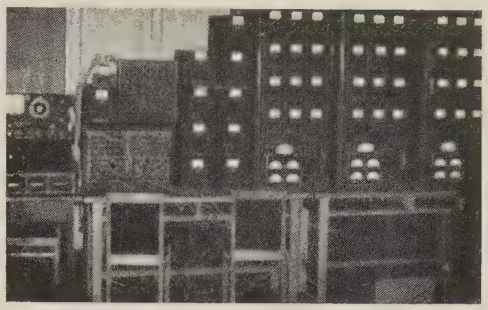


Fig. 37—MPT-9 analog computer.

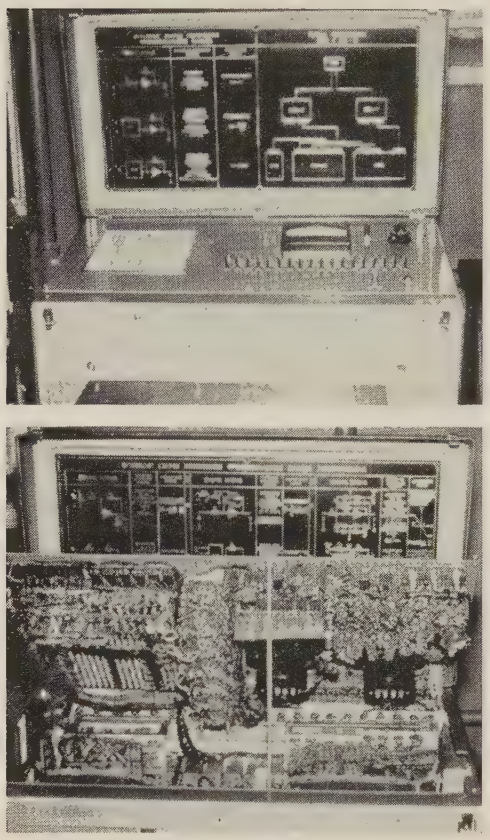


Fig. 38—MN-M analog computer.

M-20

In deference to Academician Lebedev's desire to have the first publication of M-20 details appear in the Soviet literature, the delegation agreed to withhold publication of information about this machine until the Russian paper appears. Data on this machine will be published later as a supplement to this report.

ARAGATS, RAZDAN, YEREVAN

These three machines are under development at the Institute of Mathematical Machines in Yerevan, Armenia. The delegation was unable to arrange a visit to this facility, although S. N. Mergelyan, when visting the United States, gave some details of these machines. The ARAGATS, based on a statistical distribution of 25 per cent multiply and 75 per cent add, is reported to be a 15,000 operations per second vacuum tube ma-

chine. One is to be delivered to the Computing Center at the University of Leningrad in approximately one year.

The RAZDAN is to be the first all-transistor machine in the Soviet Union and is to have a speed of from 4,000 to 6,000 operations per second. It was thought by IPMCT workers that all of the circuit development work necessary for this machine would be done at Yerevan and would not draw on the work at Moscow.

The YEREVAN is said to have a highly-developed logic and instruction repertoire, although it is the slowest of these machines, having a speed of 2,000 operations per second. It is to be a vacuum tube machine.

These three names are respectively a mountain, a river, and a city in Armenia. According to an article in an American Russian language newspaper, these three machines are all to be completed in 1959. This same article quoted the addition time of the ARAGATS as 5 μsec.[22]

LEM-I

This machine was not seen by the delegation, although the Director of the laboratory in which it was built, Professor L. I. Gutenmakher, did meet the delegation and discuss his work at some length. A reference to the machine is included here in order to call attentio to the availability of an English translation of an artic partially describing the machine.[23]

EV-80 (Fig. 39)

This machine, built in 1950, physically resembles t 604 punched card calculator produced in the Unite States. The electronic component is very similar in d sign, but the card device contains three card fee rather than the one of the U. S. machine.

Punched-Card Equipment

Some of the older models of Russian punched ca equipment were seen at the Academy of Sciences, Mo cow Computing Center. We saw a key punch (Fig. 4 and a verifier (Fig. 41), each of which looked very muc like earlier model United States counterparts. We al saw a machine for comparing cards. It operates at 4 cards per minute and at the Computing Center w usually used to compare the outputs of two STREL runs of the same problem. The tabulator (Fig. 42) o erates at approximately 100 cards per minute, and h 70 numeric positions for printing. It also has an 8-pos tion multiplier and 80 counter positions. The tabulat uses a key punch as its summary punch. We also saw

[22] See: Novoye Russkoye Slovo for Wednesday, May 20, 1959. The article is a partial reprint of an original article appearing in a Soviet teenage magazine, "Ogonek." The information from this source was made available by Mr. Eugene Zaitzeff of the Bendix Systems Division, Ann Arbor, Mich.

[23] Yu. A. Machmudov, "The LEM-I, small size general purpo digital computer," *Radio Technika* (*Moscow*), pp. 47–57; March, 195 Also published in *Commun. Assoc. for Comp. Mach.*, vol. 2, pp. 3– October, 1959. A translation of this article is also available from t Office of Technical Services, Dept. of Commerce, Washington 2 D.C., Document No. 705-D.

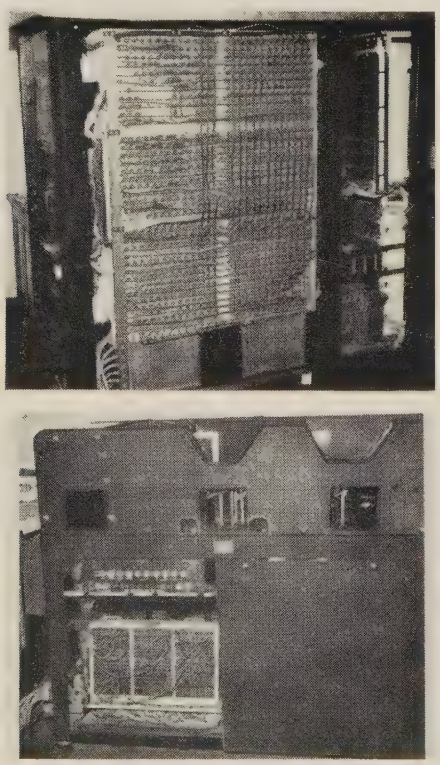


Fig. 39—EV-80 calculator.

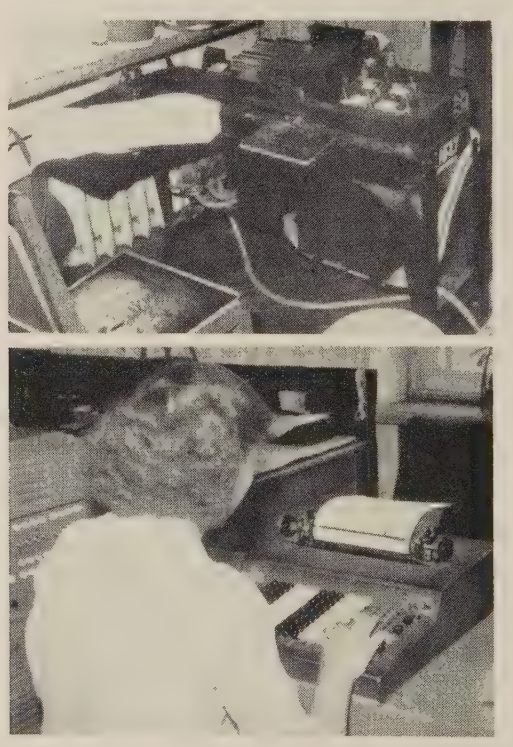


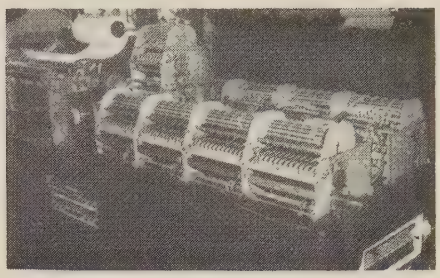
Fig. 40—(*Top*) key punch; (*bottom*) keyboard-card translator.

rd sorter (Fig. 43) which resembles its United States unterpart and operates at approximately 300 cards r minute. Fig. 44 shows a desk calculator.

est Equipment

In most of the laboratories and computing centers hich we visited we saw one or both of two common cilloscopes. The model IO-4 (Fig. 45) has a pass band

Fig. 41—Card verifier.



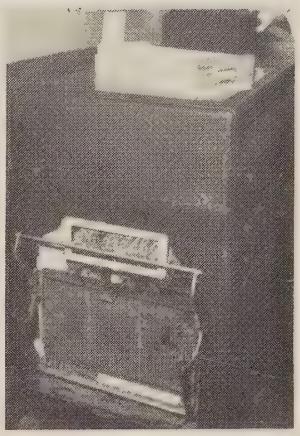


Fig. 42—Tabulator.

Fig. 43—Card sorter.

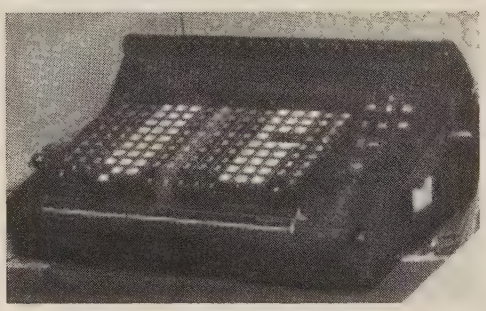


Fig. 44—Desk calculator.

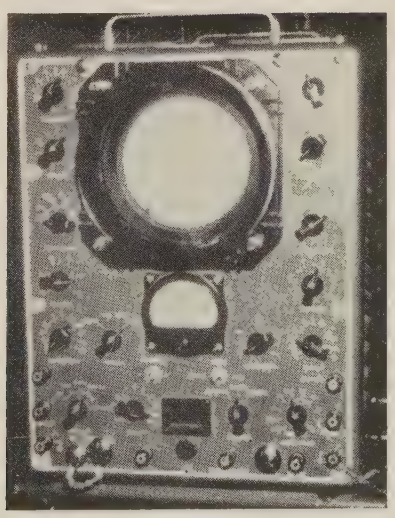


Fig. 45—Model IO-4 oscilloscope.

from 20 cycles to approximately 6 mc. It consists of two boxes and usually is mounted on a dolly. The model DESO-1 oscilloscope is a twin-beam unit; one of its amplifiers has a response from approximately 200 cycles to 80 mc, and a guaranteed rise time of 15 mμsec, but a gain of only 100. Its fastest sweep is 0.3 mμsec across the face of its 5-inch tube, so that this equipment is capable of resolving approximately 5 mμsec. Curiously, a small voltmeter is included on the front panel to monitor the ac line voltage. We were also told that oscilloscopes with pass bands of 200 mc and a rise time of 5 mμsec were production items. It appeared that their oscilloscopes generally did not have a pass band down to 0 cycles.

Other Machines

A number of other machines, some of them special purpose, have been referred to in Soviet literature and by members of their delegation. Mention of them is made here simply to indicate their existence and the scope of the Soviet computer activity. None of these machines was seen by the American delegation, nor is much information available.

VOLGA	General purpose, not yet completed.
POGODA	Special purpose, weather prediction.
KRYSTAL	Special purpose, crystallography problems.
GRANIT	Special purpose, statistical problems.
M-2	These two machines are general purpose, and are associated with I. S. Bruk; he is associated with either a different laboratory of the Academy of Sciences or an industrial design bureau.
M-3	
LUCH	Thought to be general purpose, and constructed at the Institute of Physics and Mathematics of the Belo-Russian Academy of Sciences.
M-50	Thought to be in the final stages of design and construction; likely to be a follow-on to the M-20.

General Development of Machines

We accumulated fragmentary information which indicates in part how the Soviet Union controls research. Subordinate to the Council of Ministers is, among other organizations, the Academy of Sciences, GOSPLAN (State planning committees), and the Ministry of Higher Education. Each of these can conduct research either on its own initiative or on request. The work at Moscow State University, for instance, is within the Ministry of Higher Education, while the work at IPMCT is within the Academy of Sciences. The Institutes of the Academy are sometimes specialty-oriented (IPMCT—computers) and sometimes task-oriented (VINITI—information dissemination). In the event that a laboratory of a university and a laboratory of an Academy institute happened to fall into competition in some area, the decision to resolve, to fund, or to control this parallel effort would need to be made in the Council of Ministers.

Decisions related to the production of computers and perhaps to designated research toward new ones are evidently made in the planning committees of GOSPLAN and perhaps in the State Scientific-Technical Committee attached to the Council of Ministers. The personnel of an Institute may participate in the activity of these bodies although the Institute itself does not cast such decisions.

The Institute of Automation and Telemechanics is organizationally in the Department of Technical Sciences of the Academy; the Steklov Institute, the Moscow Computing Center, and the Institute of Precise Mechanics and Computing Techniques are in the Department of Physico-Mathematical Sciences. The two universities are organizationally in the Ministry of Higher Education. There are numerous other Institutes of these two departments of the Academy, and there are several other departments. In addition, there are research institutes attached to GOSPLAN, to other All-Union Ministries, and to various state committees. It is quite possible that computer developments are in progress in some of these areas; the contacts with the western world in computing matters have been almost exclusively through Lebedev and his Institute.

Applications

Machine Translation of Languages at Leningrad

At Leningrad University a group of eighty people is working on machine translation. This Experimental Laboratory of Machine Translation is headed by Dr. Nicoli D. Andreyev, and includes S. Ya. Fitialov of the Leningrad University Computing Center and G. C. Tseiten,[24] a logician. Research on translation by automatic means is also done at three places in Moscow, at Kiev, at Yerevan, and at Gorki.

They have separated the problem into analysis and synthesis. Under analysis is included several steps of which only morphology and syntactical analysis have yielded to their studies. Morphology is the identification of a word in a dictionary plus its declension or conjugation; they feel that they have a solution to this. Syntactical analysis is difficult in Russian because the word order is freer than in English.[25] Fortunately, they have found that scientific Russian is not so varied in its syntactical structure and consequently they feel that they can handle its analysis. Since the other problems of analysis have not been solved, nothing has yet been done on the problem of synthesis.

A conference on mathematical linguistics has been held recently at the University of Leningrad and a Proceedings is expected to be published. The Leningrad group has already published one book on the subject of machine translation and hopes to publish two more in 1959. They also told us of a very complete three-volume Russian grammar which has been published by the Soviet Academy of Sciences.

[24] Name uncertain. This may be M. L. Tsetlin, referred to previously, or it may be G. S. Tseytin.

[25] In addition to translating other languages to Russian, the Soviet research effort also includes the translation of Russian to other languages; hence the great interest in Russian syntax. There is no known research in this country interested in translating English to any other language.

achine Translation of Languages at the Institute of Pre-se Mechanics and Computing Techniques

The language translation work at this Institute began 1954, and an algorithm adequate for initial experi-ents was completed by May, 1955. For the first experi-ent on BESM-I, three English books of 400 pages each ere analyzed and a dictionary of approximately 2000 tries was hand compiled. The algorithm for this ex-riment contained approximately 12,000 3-address in-ructions. In this first experiment the machine routine nd the vocabulary were contained in the magnetic rum and tape stores.

Their English dictionary has grown to approximately 500 entries and each experiment processes approxi-ately 2000 sentences. An algorithm exists for analysis English grammar and they have developed a dic-onary for the Chinese-Russian work. The Japanese-ussian work is just starting, but a dictionary for words aving a single meaning and the analysis algorithm al-eady exist. The groups working on the various lan-uages work separately but exchange their ideas and echniques freely.

The IPMCT group presently feels that a dictionary approximately five to six thousand entries of techni-l terms is sufficient for one complete area such as athematics. They also feel that approximately 45 per ent of the content of a technical article will be words ot peculiar to the technical area. Therefore, a total ictionary of approximately 10,000 entries is felt to be fficient for most work. They anticipate that for some me as much as five to ten per cent of the words in a ew article will not be found in a dictionary of this size.

Although their initial work used "binary" algorithms hich proceed directly from the source language to the arget language, they now feel that it is desirable to anslate the source language into an intermediate nguage from which an exit to any desired target lan-uage can be made. In this connection Mrs. Nikolayeva nd Bobitskiy[26] are attempting to construct algorithms r translating Russian into an intermediate descriptor nguage. Such an intermediate language would estab-sh for each word in the source material a set of descrip-ve characteristics which define the use of the word and s context. In this connection their sentence structure nalysis algorithm first identifies the stem of each word nd then identifies any endings, prefixes, etc., which ay be present. The next step of the algorithm identi-es clauses, phrases, and word groups and also tries to esolve these structures. By consulting the dictionary at ach step they also establish grammatic features for ach word. So far very little progress has been made in onstructing the synthesis algorithms which reconstruct he material in any desired target language.

Present experiments still use the BESM-I which is a miting factor. The lack of alphabetic input-output facilities on this as well as on other machines is a serious limitation to actual machine verification of the algorithms. N. L. Korolev, who took part in the early experiments, indicated that he felt a special machine for language translations might be about as follows:[27]

1) An input character reading device based on some simple logic.
2) A large read-only store of perhaps 100,000 words for the dictionary and a large part of the routine.
3) A small internal operating store of perhaps one or two thousand words.
4) Simple logical instructions not necessarily including alpha-numeric capability. The logic would probably use a Boolean algebra of two arguments.

Some of the algorithms which have been written utilize tables. In particular, the IPMCT group uses an idiom table and marks any word which might be part of an idiom. Preposition tables which relate classes of words to meanings of prepositions are also used.

Information Retrieval

The Laboratory for Electro-Modeling, directed by Professor L. I. Gutenmakher (Fig. 46), is approxi-

Fig. 46—Professor L. I. Gutenmakher.

mately 21 years old, having first been organized in 1939. At that time the function of the laboratory was the analog modeling of physical phenomena. In 1945 the goals of the laboratory were redirected, and in 1953 the most recent objectives were stated to be the modeling of mental processes and of the brain. The first efforts will be directed to mechanizing such logical mental processes as reading and abstracting. At present, this Laboratory includes the following groups:

1) A logical-mathematico department,
2) A mathematical linguistics department,

[26] This may be Barbitskiy.

[27] The LEM-I at Gutenmakher's Electro-Modeling Laboratory has many of these features. It may be an experimental special machine to test language translation concepts.

3) A department of mechanical methods in chemistry,
4) A department of storage devices,
5) A department of permanent and erasable stores,
6) A department of machine elements,
7) A department of machine exploitation,
8) A department of analog electrical modeling.

Professor Gutenmakher felt that the problem of mechanizing automatic abstracting consists of three parts: first, obtaining visual characters in some coded form; second, storing this information in some efficient form; and third, forming the abstract, which is thought to be the most difficult part. He felt that special purpose rather than general purpose machines are desirable. For this reason the LEM-I machine was constructed to test components developed in this laboratory and to investigate some techniques for information retrieval and perhaps machine translation.

This Laboratory has developed a form of read-only store which utilizes sheets of paper on which small capacitors have been printed.[28] It was stated that 100,000 bits of this capacitor storage is now operating in the laboratory and that the store is now ready for production by industry. In this store, data are retrieved on the basis of a descriptor rather than on the basis of a direct address. Thus simulation of the characteristics of such a store on a conventional general-purpose machine is difficult and ineffective for their experiments. Although the store responds to a descriptor rather than an address, it still contains a fixed word length for each descriptor. Professor Gutenmakher indicated that his laboratory is working on algorithms and equipment for information retrieval and that it has already developed an algorithm for describing an associative store. This algorithm resembles those which are being developed for machine translation. This Laboratory is also independently developing magnetic elements for their special machines. Magnetic elements will be used because of the requirement for reliability.

The work of the Laboratory for Electro-Modeling appears to parallel the work in the United States on the use of heuristic techniques in information processing. Professor Gutenmakher felt that what he called the associative technique was another way of describing the heuristic approach. He also indicated that they have now given up trying to describe the activity of mental processes by partial differential equations.

Rakov, a colleague of Gutenmackher's, has constructed a punched card information retrieval system which can scan 400 abstracts per minute. Each card in the file has from one to 24 descriptors associated with it.

Apparently the Laboratory for Electro-Modeling a one time was organizationally part of the Institute fo Precise Mechanics and Computing Techniques, but wa transferred to the Institute for Scientific Information It is uncertain whether the laboratory still has thi status or exists as an independent organizational entity in the Academy of Sciences.

Character Recognition

Work on character recognition is being done at th Institute for Precise Mechanics and Computing Techniques, but there was no discussion of this subject. A the Steklov Institute, Dubinsky is working on the ide of drawing a series of parallel lines through a line o print and then attempting to identify the characters b examining the intersections of the series of parallel line with the letters. We did have an extensive discussio about the character recognition research at the Com puting Center at Kiev.

One technique was demonstrated and discussed b Kovalevskiy (Fig. 47) and Pukhov. The technique is a

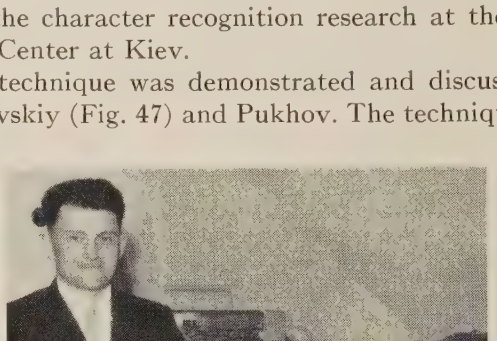


Fig. 47—Kovalevskiy and experimental character reading device.

edge-tracing scheme in which the beam of a cathode-ray tube scanner moves either clockwise or counter-clockwise depending on the output of a photo cell which views the reflection from the 1-inch high character under test. The scan is arranged so that after it has moved 0.1 inch in a straight line, it seeks to determine whether it is in a black or white area. If black, the beam turns perpendicularly in a counter-clockwise sense and continues to scan for another 0.1 inch. If white, the beam turns perpendicularly in a clockwise sense and scans for the next 0.1 inch. Therefore, the beam tends to follow the outline of the character. In order to assure stability of the edge-following, the scan is arranged so that if a transition from black to white occurs in the first half of a 0.1-inch increment, the length of the next increment is made shorter. On the other hand, if the transition from black to white is found in the second half of the step, the following increment is made slightly longer. It is intended that the pattern information generated by this scan will be stored in a computer and from it wil

[28] J. W. Carr, A. J. Perlis, and J. E. Robertson, "A visit to computation centers in the Soviet Union," *Commun. Assoc. for Comp. Mach.*, vol. 2, p. 11, June, 1959. 2) *Avtomaticheskoye Upravleniye i Bychislitenaya Tekhnika*, Moscow, p. 136; 1958. Available translated from the Office of Technical Services, Dept. of Commerce, Washington 25, D. C.; JPRS: S-871-N, 50 cents. 3) A. Kent and I. S. Isbell, "Soviet documentation," *Amer. Docu.*, vol. 10, p. 13; January, 1959. Contains pictures of the storage device.

computed the average direction of the line, quantized the nearest 45 degrees. It is believed that a sequence such quantized line directions will then characterize h character. When the scanning reader is actually nnected to a computer, it may be necessary for the mputer to control the motion of the scanning beam the basis of previous history.

A more elaborate concept suggested by Glushkov in-ves the scanning of a square in order to determine average darkness. The beam would be programmed scan adjacent squares in order to determine the direc-n of maximum darkness and to move in that direc-n. The associated logical equipment would store this rection and control the motion of the beam accord-gly. The direction and curvature of motion would then computed using first and second differences. A large ange of direction would indicate that such an inflec-n point should be recorded. If necessary, a coarse easure of length, such as short, average, or long, will o be computed for each line segment. It is hoped that om such a scanning scheme, a set of invariant char-teristics can be determined for each character. Ini-lly they intend to utilize approximately 50 words of orage, and it was thought that the associated logic ould be constructed in terms of inexpensive magnetic re components.

eory of Human Memory

Linkovsky (Fig. 48), an engineer who has worked in th applied and pure mathematics, formulated a the-

Fig. 48—G. B. Linkovsky.

y of the memory function in the human brain several ars ago.[29] He conjectures that the memory function the brain is supplied by a collection of nonlinear cillators. Experiments have shown that there are two autonomous memory systems possible, one of which preserves the pulse amplitude as it is (relative memory) and the second of which quantizes the height (absolute memory). He believes that the memory function in the brain is of the absolute kind. He argues that a nonlinear oscillator can operate in two fashions: relatively, by integrating sets of pulses, or absolutely, by merely repeating any pulse form which comes to it. Such an oscillator will oscillate if the duration of the excitation pulse τ' is less than the lag time of the circuit τ in the following equation:

$$x(t) = A[x(t)]x(t - \tau),$$

and if A is of the proper form. For A of the form

$$A(x) = \sum_i a_i x^i(t),$$

the system will oscillate if the initial value is a solution of the equation

$$A(x) = 0.$$

Initial values which are step functions of a size equal to the real roots of the polynomial equation

$$A(x) = 0$$

are solutions. Further, combinations of such pulses of height equal to the real roots will also be solutions.

A pulse consisting of the sum of three pulses of durations τ_1, τ_2 and τ_3, and each of whose amplitudes is a solution of $A(x)=0$, will be remembered so long as $\tau_1 + \tau_2 + \tau_3 < \tau$. In this context, the roots of $A(x)$ are essentially eigenvalues. For a discrete delay line of the type which this theory postulates, only signals of eigenvalue amplitude can be accommodated. Therefore, the quantized and stored wave shape cannot degrade with time except through accidental discrete jumps which means that the memory function is very reliable. As the polynomial $A(x)$ degenerates to a constant, the system becomes the conventional delay line capable of storing a signal of any amplitude, and therefore representing absolute memory.

Linkovsky estimates that the nervous system has 14×10^9 such nonlinear oscillators. Each sense organ quantizes the information which it receives into pieces that can be remembered. A signal whose duration is greater than the maximum permitted by the eigenvalues of the polynomial $A(x)$ is automatically distributed over several such memory oscillators. He believes that a repeated stimulus can cause static changes to take place in nerve cells and therefore some parts of the brain may have static memory; the brain as a whole, however, exhibits both static and dynamic memory. He concludes that since natural systems tend to be discrete and that since his theory can explain a discrete memory, the natural system may be a complete system of memory. His belief is that the nerve fibers form feedback loops and with the synapses permit the nonlinear oscillations.

[29] The journal containing this work is uncertain. It may be the *moirs of the Popov Society* or the *Journal of the Institute of Bio-sics;* publication may have been in 1955, or may not yet have oc-red.

Weather Forecasting

At the time of our first visit to BESM-I, a weather problem was on the machine. The particular model in use had been developed by Dr. Bugaev, the Director of the Weather Forecasting Institute in Moscow. The model uses 500 lattice points and is for the northern hemisphere. It predicts the pressure and vorticity pattern of the 500-millibar level. Twenty minutes of machine time is required for a 24-hour forecast.

Digitally Controlled Machine Tools

In the STRELA location at the Computing Center of the Academy of Sciences in Moscow, there was a unit capable of providing X, Y, and Z coordinates for positioning of a machine tool. Simple parabolic interpolation is used but the over-all accuracy of control is limited by the machine rather than by the computation. It has not yet been decided whether all of the tapes necessary for industrial use will be computed at a central location, or whether each plant will contain its own computation facility.

A picture of the tape unit for this experimental work is shown in Fig. 49.

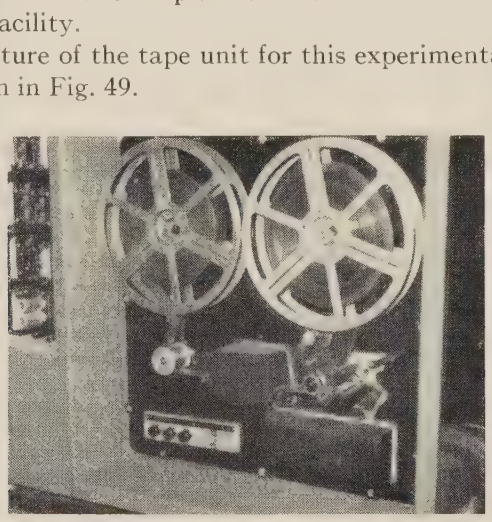


Fig. 49—Transport for 35-mm magnetic tape.

Automatic Programming[30]

The first automatic programming system for the STRELA was completed in 1955. In 1956 one was completed for the BESM-I, and in 1957 one was completed for the STRELA-III at the Academy of Sciences Computing Center. Finally, in 1958 an automatic programming system for the STRELA-IV at Moscow University was completed. Each system required approximately nine man-years of effort. The lack of alpha-numeric input-output devices has handicapped Soviet progress in this field.

Interchange of routines for the STRELA machines has been difficult or even impossible because each installation has changed the machine to suit itself. Th same situation also prevails for a number of URAL machines. Therefore each center has had to construc its own automatic programming system. Some peop in the Soviet Union feel that it is not yet time for the to standardize on a machine language. Their intent is t design many computers and to produce enough of eac one to accumulate a substantial body of experience. I perhaps five years, they believe it will be possible to s lect the best one for large-scale serial production. Mean while, translations of United States papers dealing wit FORTRAN, FORTRANSIT, UNICODE, IT, an ALGOL are being prepared and disseminated to in terested users.

Orbit Calculations

Preliminary orbit computations have been done a the Computing Center of the Academy of Sciences i Moscow although final calculations are done elsewher These calculations were done on existing serially pro duced machines rather than on machines constructe especially for the purpose; however, the machines ar specially organized.[31] There are special organization which perform the orbit calculations although th Steklov Institute is sometimes involved in the prelim inary design of the computing routines.

Some orbit calculations apparently have also bee performed by Shura-Bura at Moscow University Com puting Center although they are concerned about th accuracy of the calculations and insist that only rada data is available as input. There was considerable in terest in the question of the transmission of data ove long distances.

Linear Programming

A particular transportation problem was describe to us. It involved the distribution of building sand by fleet of trucks operating from eight sources and deliver ing to 100 sites in the Moscow area. The problem wa first solved by the Simplex Linear Programming metho and required approximately three hours on STRELA A new method was evolved which produced a solutio in approximately 30 minutes. This work was don jointly by the Computing Center and the Institute o Complex Transport Problems; the actual work on th 8×200 matrix was done by Yu. A. Oleinik. A paper o this new technique is in process. Some linear program ming work is also being done for the Institute of Rai way Transportation Problems.

Numerical Analysis

Although work on electronic computers started in th Soviet Union a few years later than in the United State the Russians have a long established tradition of ou standing work in numerical analysis. This is due partl to the strong development of applied mathematics. Th

[30] J. W. Carr, A. J. Perlis, and J. E. Robertson, "A visit to computation centers in the Soviet Union." *Commun. Assoc. for Comp. Mach.*, vol. 2, p. 11; June, 1959. 2) "Status of Digital Computer an Data Processing Development in the Soviet Union," *ONR Symp. Rept.*, ACR-37, Washington D. C.; November, 1958. 3) A. P. Yershov, "Automatic programming in the Soviet Union," *Datamation*, vol. 5, pp. 14–20; July–August, 1959.

[31] This may imply special input-output devices, or it may imp a group of machines netted by communication links.

iet Union is currently making a strong effort to
er numerical analysis as a part of the intensive de-
pment of computing. Approximately 40 per cent
he mathematical students at Moscow University
ialize in numerical analysis although the Chair of
nerical analysis is only four years old. This was
eved in part by raising the stipend for students in
nerical analysis and by lowering the academic re-
ements for maintaining this fellowship.[32] All mathe-
ics students, regardless of their specialization, are
uired to take courses in numerical analysis and pro-
mming and to have some practical experience with
puting machines.

he quality of the work in numerical analysis in the
iet Union is impressive. The group at the Academy
nputing Center has been applying a method orig-
ed by Dorodnitsyn for solving boundary value prob-
s in difficult configurations. The method consists of
lacing the partial differential equation by a system
rdinary differential equations. Although restricted
wo-dimensional problems, it is applicable to a wide
s of linear and nonlinear situations. In the detached
ck wave problem, Dorodnitsyn's method appears to
the only approach in which the solution starts from
geometrical outline of the given body rather than
n an assumed shock wave front. The method is semi-
irical and complete theoretical justification of the
thod has been sidestepped in favor of the achieve-
nt of practical results.

At Moscow University the research in numerical an-
sis centers in Lusternik, Berezin, Zhidkov and
olev. In Lengingrad, Ladyzhenska has developed a
thod for solving differential equations using large
s while simultaneously achieving small errors.
ntorovich, who is one of the discoverers of the linear
gramming technique, is going to the Novosibirsk
entific Complex where a strong development in com-
ational mathematics is expected. Russian work in
nerical analysis is published in a special journal.

he Russians seem to have succeeded in attracting
re of the powerful theoretical mathematicians into
nerical analysis and computational mathematics
n has the United States. The intellectual climate in
ssian mathematics makes it easier for an abstract
thematician to make valuable contributions to ap-
d problems. Related fields in mathematics such as
ne theory and cybernetics were at one time under a
ud of ideological suspicion, but this has now been re-
ved and many prominent Russian scientists are en-
ng these fields.

Circuits and Components

in Films

he development of thin film magnetic devices ap-
rs to be in its early stages. We were shown experi-
mental vacuum evaporated deposited film samples on glass plates. These films were circular in shape, had been deposited at a pressure of 10^{-4} to 10^{-5} mm of mercury at a temperature of 200° to 500°C, and were permalloy (80 per cent nickel and 20 per cent iron). The films were from 500 to 2000 Å thick and exhibited an exceptionally square hysteresis loop. They ultimately hope to achieve a switching time in the order of 20 to 50 mμsec.

The experimental setup for determining the hysteresis loop at 50 cps is shown in Fig. 50. This arrangement permitted placing the sample film in a uniform magnetic field on a table which could be rotated to orient the sample with respect to the field. Compensating coils were provided to adjust for field nonlinearity. Surrounding the solenoid which generated the uniform ac field was a rectangular wire frame through which direct current could be passed to rotate the direction of the uniform field.

Kobelev indicated that they were not presently doing any low temperature thin film experiments at IPMCT, but that such work was being done elsewhere.

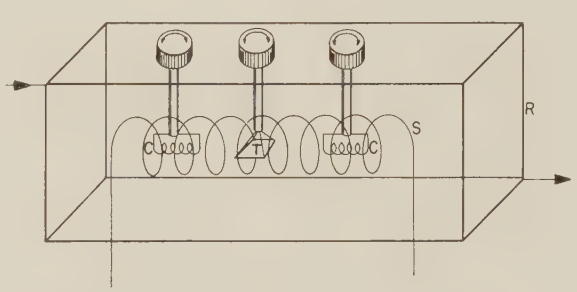


Fig. 50—Experimental setup for determining 50-cycle hysteresis loops of thin magnetic films. S = solenoid for generating uniform ac field; T = table to hold sample (rotatable); R = "external" cubic frame for rotating field; C = compensating coils (B-H pickup coils not shown).

Ferrite Cores

An experiment was demonstrated for investigating the switching time of magnetic core materials. The particular sample shown was being switched at a 100-cps rate, in a coincident current mode at 0.5 μsec. The rise time of the current pulses was approximately 10 mμsec; with increased drive the same cores could be switched at 80 mμsec. Under these conditions the switching field was the order of 5 to 6 oersteds. The cores were approximately 3 mm in outside diameter and the H_c was approximately 1 to 2 oersteds.

We also saw in operation equipment for automatic testing of cores. It is similar to that which is used in this country for the same purpose.

A detailed discussion of the characteristics of some magnetic cores which were given to the delegation is contained in Appendix III.

Transistor Circuits

Transistor circuits were demonstrated using industrially produced P-N-P alloy diffusion transistors with

[32] These special inducements for students in numerical analysis e recently been abolished.

a 120-mc alpha cutoff. 400-mc transistors are available but are in use only in communication circuits. In one laboratory we observed an experiment for determing optimum characteristics of transistor triodes by the systematic determination of the small current breakdown voltage. For the 120-mc transistor, typical reverse current is 5 μa at a reverse base-emitter voltag of two volts.

A flip-flop was demonstrated which exhibited a 2 mμsec rise time and was changing every 200 mμsec. Th transistor logic circuits which we saw utilized the cu rent switching OR and AND configurations; an excl sive-OR version also exists.

We also observed a ten-stage transistor-core shi register packaged in a plug-in unit. They have exper enced no particular difficulties with the contacts of Jones-like plug. The frame into which these particul packages were inserted was also shown (Figs. 51 and 52 Fig. 53 shows the schematic of the SETUN ternary shi register.

The characteristics of sample transistors which wer given to us are shown in Fig. 54.

Miscellaneous

The engineers in charge of machine development a the Institute of Precise Mechanics and Computing Tech

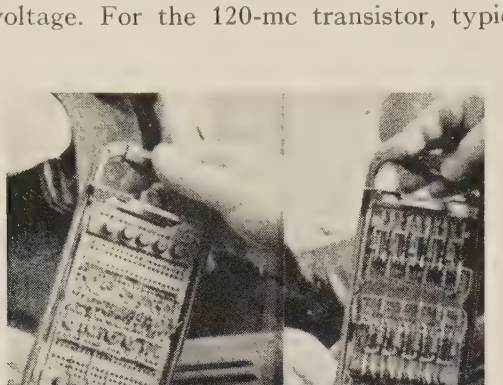


Fig. 51—Pluggable transistor package.

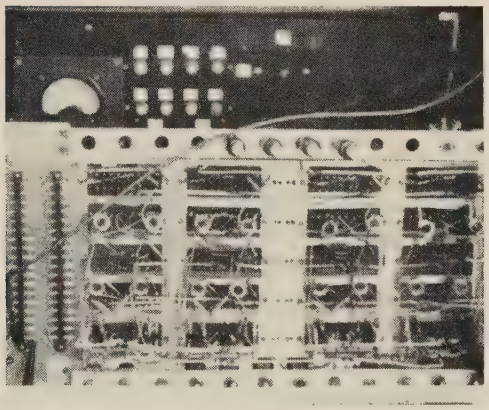


Fig. 52—Mounting frame for transistor packages.

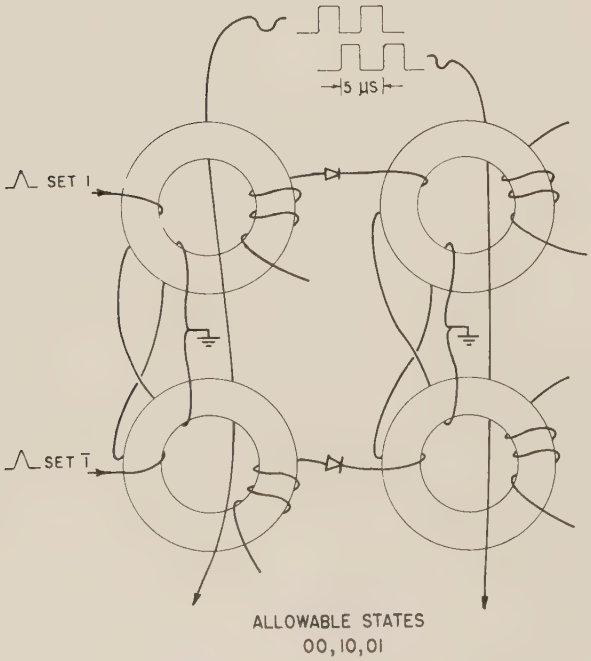


Fig. 53—Schematic of SETUN ternary shift register.

I. [2,4]Germanium high-frequency transistor, type P403A (experimental sample)

Collector voltage[1]	−5 volts
Emitter current[1]	7.5 ma
Current amplification	>0.96
Oscillation frequency[3]	> 120 MC
Collector capacitance	< 10 mmf
Collector reverse current	< 5 μamps
Output conductance	< 5 μmhos
Collector capacitance × base resistance	< 500 $\mu\mu$f-ohms[6] (μsec)
Type	PNP

II. [2,5]Germanium junction transistor, type P406 (production sample)

Envelope marked:
Russian Socialist Federative Soviet Republic
Leningrad Council of the National Economy (LSNKH)
Administration of the Radiotechnical Industry

Collector voltage[1]	−6 volts
Emitter current[1]	1 ma
Current amplification	>0.95[1]
Current amplification at 10 mc	>0.70
Collector capacitance	< 20 mmf
Collector reverse current	< 6 μamp
Collector capacitance × base resistance	<2500 μsecs[6]
Collector dissipation (natural cooling)	30 mw
Maximum case temperature	75° C.
For common emitter circuit:	
Collector potential	−6 v
Collector current	< 5 ma
Type	PNP

Solder at least 5–8 mm (0.2–0.3 inch) from case for not more than 2–3 seconds with a 50–60 watt iron.

[1] It is not stated whether these are maximum or typical values.
[2] This is a translation of the information on the envelope in which the transistor came.
[3] This is very clearly an oscillation frequency (GENERATSIY CHASTOTA) and not an α-cutoff frequency.
[4] The only source information on this envelope is GKRE-Scientific Research Institute. This is thought to be the State Committee for Radio-Electronics Scientific Research Institute.
[5] This transistor almost certainly comes from the Svetlana Tube Plant in Leningrad.
[6] The use of a different form of unit here plus other differences in the original information clearly suggests these two transistors come from different organizations.

Fig. 54—Transistor characteristics.

ues indicated that the recombination time of the best sian diodes is 0.1 μsec. With the uncertainty in the nition of the term itself, it is not clear whether this pares favorably or not with the best presently ilable diodes in the United States. There seems to be e interest in the Soviet Union in developing spe- ized beam switching tubes for purposes of logical ration rather than storage. Soviet standard radio or vision tubes exhibit an average life of 5 to 10 thou- d hours and therefore it has not been necessary to elop special long life types for computer usage.

oviet design philosophy appears to parallel that in country. They derate the current capability of es by 50 per cent. They also derate the power rating esistors by 50 per cent, but, in general, they operate acitors at 100 per cent of rating because their pro- tion test procedure tests the capacitor to double its king voltage during manufacture. Common resistors e a 5 per cent tolerance but occasionally they match rs for particular applications such as a voltage di- er.

Major Machine Components

gnetic Drums

ome magnetic drums appear to be in serial produc- by industry. The unit shown in Fig. 19 is used on the BESM-II machine, the Kiev machine, and was seen in other places. A summary of magnetic drum characteristics is shown in Table II. In this table the unit listed under BESM-II is the one which appears to be an off-the-shelf item of commerce.

Magnetic, Paper and Film Tapes

Early machines utilized punched 35-mm cinema film. The punched film handler of the URAL-I is shown in Fig. 25. A similar transport is also used on URAL-I to handle 35-mm magnetic film. Both tapes of URAL-I are closed loops, implying that a reverse mechanism does not exist. The perforated tape operates at $1\frac{1}{2}$ meters per second with a data rate of 75 numbers per second, and at a packing density of 50 numbers per meter. The data transfer rate on the magnetic tape is also 75 numbers per second.

The STRELA is equipped with a magnetic tape unit whose tape is approximately four inches wide. A word is written on this tape completely in parallel. Fig. 30 shows this unit.

The magnetic tape units of the BESM-I are modified audio tape transports and are shown in Fig. 14. The perforated tape reader also uses a similar transport (Fig. 15).

Table III summarizes the characteristics of the magnetic tape transports of the various machines.

TABLE II
Soviet Magnetic Drums

Drum	Speed, RPM	Diameter, inches	Length, inches	Circumferential packing, pulses per inch	Axial packing, tracks per inch	Number of tracks and heads	Capacity, words per drum	Head spacing, mils	Head gap, mils	Transfer rate, words per second	Remarks
ratory za)	1500	15–18	—	—	—	44 tracks 88 heads 2 stations	4000 bits/ track	—	—	—	—
L-I	6000	—	—	—	—	—	2048 half words	—	—	100	—
L-II	6000	—	—	100 (4 pulses/mm)	4 (6 mm between tracks)	—	8192	0.8–1 (20–25 microns)	40 (?) (1 mm)	5000	Expect 6 months with no inspection of drum; spare drum to be supplied with each machine; customers will report troubles.
M-I	—	—	—	75 (3 pulses/mm)	—	100	6000 40 bit	1.2 (30 microns)	—	—	—
M-II	1500	12 (30 cm.)	16 (40 cm.)	75 (3 pulses/mm)	10 ($2\frac{1}{2}$ mm between tracks)	44 tracks 88 heads	6000	0.24 (?) (6 microns)	—	12,000	Similar drum ran 3 years on BESM-I without trouble.
cal U. S. 1959	1800	8–12	12–36	100–400	10–20	—	8–50,000	0.25–1	0.25	10–50,000	Special drums are as large as 400,000 words with a recording density of 1000 pulses per inch.

TABLE III
Soviet Magnetic Tapes

Machine	Width	Linear Speed inches per second	Start/stop	Density bits per inch	Words per tape	Transfer rate, words per second	Tracks
SM-I	$\frac{1}{4}$ inch	—	4 seconds (?)	—	30,000 (?)		2
SM-II	$\frac{1}{4}$ inch	80 (2 m/sec)	seconds	200 (8 bits/mm)	30,000	400	2
AL-I	35 mm	30 (0.75 m/sec)	msec	32 (1248 bits/m)	40,000	75	11
AL-II	35 mm	60 (1.5 m/sec)	msec	210 (8,300 bits/m)	700,000	1000	11
RELA	4 inches	16	seconds	62 ($2\frac{1}{2}$ bits/mm)	200,000	1000	43
20	—	—	—	—	—	—	—
pical U. S. ly 1959	$\frac{1}{2}$ inch–3 inches	75	5–10 msec.	200	1,000,000 maximum	2,500–10,000	7 to 36

Input-Output Equipment

The BESM-I uses punched paper tape input and output. The BESM-II will also use punched paper tape input and output. Both machines also have a 15-line per second, 14-column numeric-only printer (Fig. 16). The STRELA uses punched card input and output. The card equipment appeared to be generally similar to that in use in this country for the same purpose although the operating rates are somewhat slower. A full line of numeric 80-column and 90-column punched card equipment is presently manufactured in the Soviet Union and such equipment will probably be coming into increasing use for input-output facilities of computers.

Two new printers were demonstrated. At Penza the the rotating drum printer intended for the URAL-II was seen. Timing signals are provided by illuminating a sequence of slots cut into the circumference of a hollow

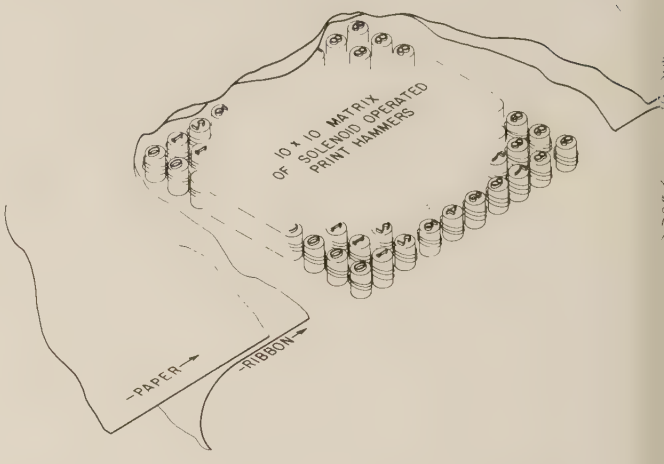


Fig. 55—Schematic of 50 lines per second printer.

TABLE IV
SOVIET PRINTERS

Machine	Columns	Characters	Printing Rate lines per second	Remarks
BESM-I	14	Numeric	15	No carbon copies; Roll paper
BESM-II	14	Numeric	15	No format carriage control
STRELA	10	Numeric	50—	Experimental, not yet completed. Roll paper
URAL-I	19	Numeric	1.6	
URAL-II	16 to 96	Numeric	20	
KIEV	19	Numeric	1.6	
Typical U. S. early 1959	up to 120	Alphanumeric—up to 56 characters	Up to 15	Fanfold paper, multiple copy, format carriage contr

cylinder at the end of the drum. The passage of the slots is read by a set of germanium photo diodes; the data to be printed are stored in a magnetic core matrix on a character-by-column basis. At the STRELA location of the Computing Center of the Academy of Sciences an experimental numeric-only printer was demonstrated. This device is not yet fully operational and it is hoped that it will ultimately achieve a rate of 50 lines per second, 10 characters per line. The principle of operation of this printer is shown in Fig. 55. As is seen from this figure, the zeros in any line are inserted at one position of the paper, the ones of the same line are inserted in the following position, and so forth. Therefore to completely print one number only, it requires 10 advances of the paper. However, in printing a long sequence of numbers, 10 lines at a time are being completed. Such a printer requires that 10 complete lines of information have to be prepared and stored within the computer. There is also a rather complicated refill and release cycle necessary to couple the printer and the machine proper.

Table IV summarizes the characteristics of the known-printers.

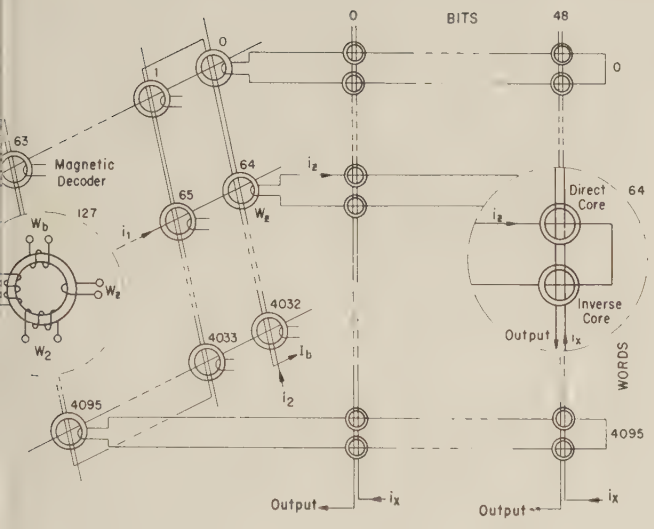
Magnetic Stores[33]

The 1024-word store designed at the Institute f Precise Mechanics and Computing Techniques h served as the model for the stores of subsequent lar Soviet machines. The same storage device is being us in BESM-II[34] and also in the Kiev machine. Contra to the usual store organization in this country, the S viet so-called type Z system is not a coincident curre read; an N-way decoder switch is used to end-drive columns of the desired word (Fig. 56). Approximate one and one-half times switching current is applied the core for reading. Writing into the store is, howeve coincident current.

In order to minimize the change in load presented

[33] V. V. Bardizh, "Magnetic Internal Memory with Direct Sele tion," Institute for Precise Mechanics and Computing Techniqu Academy of Sciences, USSR, Moscow; 1958. This paper was pr sented at the 1958 University of Michigan Summer Conference Computing Machines. See also S. A. Lebedev, "Certain Works the Sphere of Computing Techniques," Institute for Precise M chanics and Computing Techniques, Academy of Sciences, USS Moscow; 1956. This paper was presented at a 1956 conference Stockholm.

[34] Aleksei Fedorov, one of our technical guides, was largely sponsible for the design of the 2048-word version used in BESM- and other machines.



. 56—Essential features of the Type Z store. (This drawing is patterned after one in a paper by V. V. Bardizh.)

e end drive switch, two cores are used for each bit. In is way the same number of cores changes state at ch cycle regardless of the digit content of the word. ne cycle time of the standard type *Z* store is 6 μsec, though in the BESM-I and BESM-II machines, it is ed at a 10-μsec cycle. The basic unit of construction is rectangular frame which contains both storage and itch cores. Each frame contains 128 48-bit words or total of 12,288 storage cores (128×48×2), and also ntains the 128 switch cores. These frames are then acked to provide over-all stores of 1024, 2048, or 4096 ords. So far, no machine has utilized all of the 48 bits ovided. The extra bits are regarded as spares in case fabrication difficulties.

An experimental store has also been built using two res per bit and operating with a total cycle time of 0.2 ec. The cores in this experimental unit have an inside ameter of 1 mm and the current drives have a rise me of approximately 30 mμsec. There is also in serial oduction by industry a 64-word by 50-bit store with one-microsecond cycle time. It is possible that this it is not a coincident current type but rather a magetic shift register type.[35]

Experimental transistor stores have been constructed ut adequately fast high current transistors are not resently available. It was estimated on the basis of eir experience that the inductive voltage for 40 cores of the order of $\frac{1}{2}$ volt.

The magnetic core store for URAL-II is a one core er bit coincident current type.

ther Components

Typical other types of components are shown in Fig. 7.

[35] There is some uncertainty whether the cycle time is 0.3 μs or 1 . The best guess is a 1-μs cycle time but a 0.3-μs access time.

Fig. 57—Various electronic components (identified by position):
P-403A Transistor
Capacitor
P-406 Transistor
Capacitor
Wound Core
Resistor
Capacitor
Diode
Potentiometer

Education[36]

The career of a student begins with ten years in elementary and high school. All students not in the upper five per cent of the graduating class are required to have two years of working experience before applying to an institution of higher learning. A high school graduate is permitted to apply to one university only and, if rejected, cannot hope to gain admission at that time to another school. Admission to a university used to be based primarily on the result of competitive examinations. For mathematics, such an examination might cover mathematics, physics, a foreign language, Russian language, and Russian history. The average entering age of university students is 17, and approximately 90 per cent of them have government living expense fellowships.

After admission a student devotes five full years to study. During the first two years all students in a field take the same courses, but during the final three years specialize to a certain extent within the field. The program of study for each speciality is rigidly prescribed. By looking up his plan of study, a student will know in advance which courses he must take during each year, which term papers and examinations he will have in each course, and in which weeks these examinations will take place. Every student is required to take eleven terms of ideological subjects such as Marxism-Leninism, dialectical materialism, history of the Communist party, political economy, and economics. He is also required to take four terms of a foreign language and four terms of physical education. In his five years, a student will have to pass 32 oral examinations, will have to submit 36 reports, and write 9 term papers. During his final

[36] See: "Soviet Commitment to Education," U. S. Department of Health, Education and Welfare. The report of the first official U. S. education mission to the USSR; available from U. S. Government Printing Office, Washington, D. C., for 70¢.

term a student is required to write a diploma dissertation and to acquire some practical experience. Prior to graduation he is expected to take two state examinations: one in Marxism-Leninism and one in his speciality.

Each undergraduate student is assigned an advisor (teacher), although his final grade is granted by the Scientific Council of the university. The Scientific Council is also responsible for recommending a student to graduate study. During each semester, docents (associate professors) and the full professors lecture and hold recitations for the classes. The examinations are given by the assistants although a student's final examination is required to be given by his assigned teacher. During the five years of study there are examinations on four subjects each half year. Two or three months before graduation, each student is appointed to a job according to his speciality; he cannot leave or be dismissed from this job for three years. If there is no opening in his field, the university is obliged to find him a position in a related field. The appointments of students to jobs are apparently controlled by a Central Council for Production.

A research worker may lecture or may supervise a thesis but he is not permitted to teach until he has succeeded in a competition and shown competence in his field by means of publications or accomplished work. On the other hand any teacher is permitted to do research work.[37]

The content of each course is determined by the Ministry of Higher Education, though the preparation of the detailed program is done by the professors. The lectures are supposed to adhere to the prescribed content rather rigidly since the students are to be examined on everything stated in the program and on nothing else. A Russian mathematical graduate will have a shallower knowledge in each field than his American counterpart but he will be familiar with a larger number of fields. The Russian student will also be unacquainted with modern terminology and modern methods but, unlike the American student, every Russian mathematician has a three-year foundation in physics, and has been required to take a minimum number of courses in computer mathematics.

The diploma paper which a student writes under the direction of his advisor in his tenth term is approximately at the level of the bachelor's thesis in American universities. It must be publicly defended before an audience which includes the professors belonging to the relevant chair, the advisors, the referees, and any students who may wish to attend. After successfully passing his final thesis defense, a student graduates either simply or "with distinction." Then he either becomes an "aspirant" or must take a job. If he is required to take a job because of poor grades, he has little chance subsequently to attain a higher degree.

Future scientific workers are recruited from the ranks of the aspirants. An aspirant "aspires" to the first advanced degree, that of "candidate." He takes no formal courses in his three years of graduate work but must write a candidate's thesis and defend it at a stiff public examination. This candidate's thesis is written under the direction of an advisor and appears to be at a level slightly below that of a Ph.D. thesis in leading American universities. A candidate is entitled to teach at an institution of higher learning, but to achieve the rank of professor, he must generally earn the highest learned degree, that of "doctor."

The doctor's degree is also acquired by publicly defending a thesis. This thesis is written completely independently and must constitute a significant contribution to knowledge. Only a few doctor's degrees are awarded each year in the field of mathematics. Thus, while a Russian candidate is approximately between the American M.S. and Ph.D., a Russian doctorate degree is somewhat beyond that of the American doctorate.

The Role of the Soviet Academy of Sciences in the Scientific Life

The All Union Academy of Sciences of the USSR and the 15 Republican Academies of Sciences play a dominant role in the scientific life of the Soviet Union. The bulk of the scientific research work in Russia seems to be carried out by the various Institutes of the Academy. Each Institute seems to be a largely independent unit organizationally, is often housed in a single building, and is strongly influenced by the personality of the director who has two deputies, one for scientific matters and one for business matters. He is assisted by a Scientific Council consisting of the senior members of his Institute.

The scientific employees of an Institute are both professors of institutions of higher learning and graduates of universities, with or without advanced degrees. The support staff consists of technicians, clerical workers, etc. A professor working at an Institute may devote any percentage of his time to his work. For some, the Institute seems to be a secondary affair, a role corresponding to consulting in the United States. For others, the Institute is the principal job even though an institute employee may also give a course at a university.

An Academy Institute performs no direct teaching functions even though some of the employees may be aspirants who work on a candidate dissertation under the direction of a senior member of the Institute. Students required to gain practical experience may acquire it by working at an Institute. For instance, students come to the Institute of Precise Mechanics and Computing Techniques for practical experience in both the design of computers and the programming of computers. Such students not only come from all over Moscow, but from all over the Soviet Union and China, and spend three months there. An Institute may also give evening

[37] Notice the very particular sense in which the word "teacher" is used in the Russian connotation.

urses of a nature similar to the extension courses of nerican universities.

The highest class of membership in the Soviet Acady is that of Academician. The number of Academins in a given field is relatively small and fixed by law, d election to the Academy is considered the greatest nor which a Russian scientist may achieve. A member the All Union Academy receives a salary of 5000 bles per month in addition to any salary he may reve from his job. He is also entitled to an official car d to preferred housing. A member of a Republican ademy receives a salary of 3500 rubles per month. A ond class of membership is that of Corresponding ember who receives a salary half that of an Acamician. In 1946 each Academician of the All Union ademy received a "Dacha," or summer home near oscow.

e Economic Status of Scientists

In evaluating typical Russian salaries it must be reembered that the highest income tax in the Soviet nion is 13 per cent and that all other taxes are indirect. urther, medical care and certain other services are ovided cost free by the government. Living conditions e below American standards, and in all cases, the perntage of income devoted to rent is much lower than at in the United States. Remember also that while e tourist exchange rate is 10 rubles per dollar, the commercial" exchange rate is approximately 4 rubles r dollar.

For mathematicians in a research institute, university aduates start at 1050 to 1350 rubles per month, candiates at 1850 to 3000, and doctors at 3500 to 6000 rubles r month. The scale for engineers at similar Institutes slightly higher. For comparison, a charwoman reives 420 rubles per month, a chauffeur 500 rubles, an verage skilled worker 800, a taxi driver 1200 rubles, a gh school teacher from 600 to 1500, while old age pens ons range from 400 to 1250 rubles per month.

Professorial salaries are fixed all over the Soviet nion. A professor receives 4500 rubles per month plus n additional 500 if he is in charge of a Chair. If an cademician, he also receives the additional stipends reviously noted. Professors often supplement their come by consulting or part-time teaching at other niversities. If the professor is well known, such addional work is not difficult to obtain and a man may dote as much as 1½ days per week to this second job, r which he is paid at half rate. A particular individual ay have a full-time appointment at one Institute, may e working at a second job at another, and perhaps conlting for a third and a fourth. To some extent the sal-y structure of scientific workers depends on the imortance of the Institute. Mathematicians and physists are among the top levels.

It is also possible to earn additional income by author-g scientific books. The rate per page seems to depend pon the status of the author and upon the subject of e book; for a man just below the status of full Academician, a typical figure is 2000 rubles per 16 printed pages. The salary structure for programmers is shown in Table V.

TABLE V

Typical Salaries for Programmers

Status in Research Institute	Salary (Rubles per month)
Junior Scientific Worker, non-Candidate or Candidate of Sciences	1050–1350[1] 1850–2000
Senior Scientific Worker, Candidate or Doctorate	2500–3000 3500–4000[2]
Head of Laboratory, Doctorate	3500–6000
New Graduate, starting	1050
No Degree, 1 year experience	1200[3]
Degree, 1 year experience	1350

[1] An engineer in this category is from 1200–1800.
[2] In exceptional cases this may have an upper limit of 6000.
[3] This will be 1300 for industry.

The Novosibirsk Development

It is a general belief in Russia that the future of the Soviet Union is closely allied with the development of the immense and largely unexplored natural resources of Siberia. M. A. Lavrentyev is credited with persuading the Soviet Government to establish a powerful scientific center in Novosibirsk. Academicians Khristianovitch and Sobolev are the other two leaders of the Novosibirsk project.

This new scientific establishment is intended to be a nerve center for the development of Siberia. Novosibirsk itself is already a large industrial city and it is now to become the site of a large complex of scientific institutes and training centers for scientists. A new Siberian division section of the All Union Academy has been created with Lavrentyev in charge. The government has also created ten new positions for Academicians; among the new appointees are mathematicians I. N. Vekua and A. I. Maltsev, and the hydrodynamicist P. Y. Polubarinova-Kochina. Several other outstanding scientists have been invited to join the Novosibirsk Center; among them are L. V. Kantorovich of linear programming fame, and A. P. Yershov of automatic programming. It is intended to create a new university there whose rector will be I. N. Vekua. There is also planned a Siberian Mathematical Journal and a Siberian edition of the *Doklady*.

Chinese Developments

A number of Chinese engineers and programmers were observed in various laboratories during our visit. Apparently they have come to Moscow for training. It was indicated that the Chinese have developed a machine for themselves which is partly ferrite logic and partly vacuum tube logic, and which has a capability between that of the BESM-I and the BESM-II. The Chinese are also supposed to have developed a machine which is completely their own design. It operates at approximately 5000 operations per second and is presently being readied for serial industrial production.

Appendix I

URAL-I Instruction Repertoire

The information on the URAL-I machine is from a book which describes this machine and which was given to members of the delegation: "Programming for the Digital Computing Machine—URAL," by V. N. Bondarenko, I. T. Plotnikov, and P. P. Polozov, Moscow, 1957. Most of the information is from a table of instruction types in the rear of the book. Some of the explanatory notes have been supplemented by information from the text material. A block diagram of the machine (page 7 of the reference) is shown in Fig. 58. As shown in Fig. 59, an instruction is regarded as a half word. Of the address field, only $3\frac{2}{3}$ octal digits (11 bits) are used for direct addressing of the store; the remaining bit indicates whether a full word or a half word is desired. Of the operation code field, only $1\frac{2}{3}$ octal digits are used in specifying the instruction; the largest operation code can therefore be 37. The remaining bit is used to indicate that the instruction has an address part which will be modified.

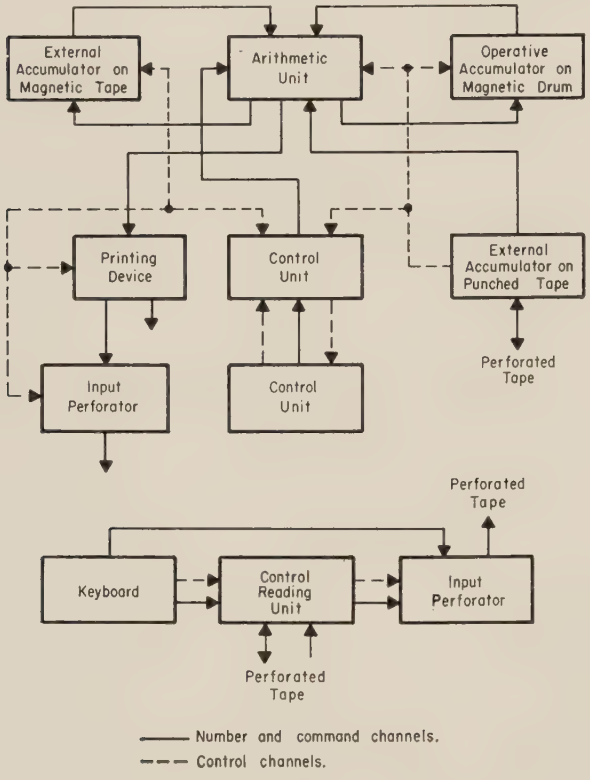


Fig. 58—Block diagram of the URAL-I.

The two signals ω and ϕ are generated within the machine under certain conditions and are used to control subsequent operations. The signal ϕ clearly plays the role of an overflow indicator; the signal ω usually plays the role of a sign indicator, although in special cases (instructions 12 and 15 for instance) it indicates other conditions. The response of the machine to these two signals depends upon the position of two console switches, the "block-ϕ" key and the "stop-on-ϕ" key. If the block-ϕ key is "on," the overflow indication is ignored, and the sequence of instructions is not changed. If the arithmetic result is less than 2, it can be normalized to less than unity without arithmetic error. If the "block-on-ϕ" key is "off," the response of the machine depends on the "stop-on-ϕ" key. If "on," the machine stops; if "off," the machine traps to storage cell 0001 in which must be stored a jump instruction to an appropriate place in the routine.

Except where necessary to clarify meaning, the Russian idiom has not been replaced by the English idiom, principally to indicate their phraseology for familiar concepts.

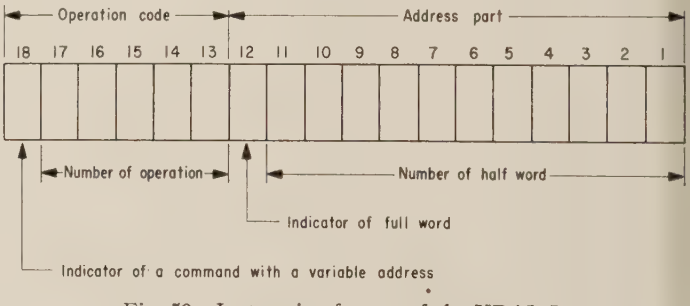


Fig. 59—Instruction format of the URAL-I.

System of Commands for the Machine URAL-I

Notation:
- (c_0) Contents of summator[1] before command has been fulfilled.
- (c) Contents of summator after command has been fulfilled.
- (p) Contents of the register[1] of the arithmetic device.
- (a) Contents of the cell a of the magnetic drum.

Number of Operations	Designation of Operations	Operation	Command (base −8)	Conditions for generation of the signals		Brief description of the operation
				$\omega=1$	$\phi=1$	
01	SL 1	Addition of numbers $(c_0)+(a)$	01a	$(c)\leq -0$	$\lvert(c)\rvert\geq 1$	$(c)=(c_0)+(a)$

[1] The word "summator" appears to play the role of our "accumulator" while "register" plays the role of our "MQ-register." The word "accumulator" appearing in the block diagram seems to imply "storage."

SYSTEM OF COMMANDS FOR THE MACHINE URAL-I (*Continued*)

Number of Operations	Designation of Operations	Operation	Command (base −8)	Conditions for generation of the signals		Brief description of the operation
				$\omega=1$	$\phi=1$	
02	SL 2	Loading a number into the summator	02a	$(c)\leq -0$	—	$(c)=(a)$
03	Vch 1	Subtracting numbers $(c_0)-(a)$	03a	$(c)\leq -0$	$\lvert(c)\rvert\geq 1$	$(c)=(c_0)-(a)$
04	Vch 2	Subtracting the absolute quantities of numbers	04a	$(c)\leq -0$	—	$(c)=\lvert(c_0)\rvert-\lvert(a)\rvert$
05	Um 1	Multiplication of numbers $(p)\cdot(a)$	05a	$(c)\leq -0$	$(c)\geq 1$	$(c)=(c_0)+(p)\cdot(a)$
06	Um 2	Multiplication of numbers $(c_0)\cdot(a)$	06a	$(c)\leq -0$	—[2]	$(c)=(c_0)\cdot(a)$
07	DL	Division of numbers $(c_0)\div(a)$	07a	$(c)\leq -0$	$\lvert(c)\rvert\geq 1$	$(c)=(c_0)\div(a)$
10	F3	Set the sign of (c_0) to the sign of the number (a)	10a	$(c)\leq 0$	—	$c=\lvert(c_0)\rvert$ with the sign (a)
11	Sd	Shift of a number	11 0000	$(c)=+0$	—	Shifting of (p) by (c_0) places; if $(c)<0$, to the right; if $(c)>0$, to the left. (c) must be in columns 19 through 35.
12	Vd	Extracting part of a number with the aid of a number (a)	12a	$(c)=0$	—	Separating the part according to the rule of column-by-column logical multiplication of (c_0) and (a). The result is (c).
13	Fr	Forming a number from numbers (c_0) and (a).	13a	$(c)=+0$	—	Forming of (c) according to the rule of column-by-column logical addition of (c_0) and (a).
14	Sr	The comparison of numbers (c_0) and (a)	14a	$(c)\neq(a)$	—	Comparison of (c) and (a) according to the rule of column-by-column addition (i.e., exclusive-OR). The result if (c).
15	Nr	Normalization of a number (c)	15a	$(c)=0$	—	After normalization, the number is sent to the cell (a). The number of shifts is placed in the summator with the appropriate sign: —if shifting has been to the left, + if shifting has been to the right.
16	Pb	Store a number (c_0) into the cell (a)	16a	$(c)\leq -0$	—	$(a)=(c)$
17	Pr	Loading a number (a) into the register	17a	$(p)=+0$	—	$(p)=(a)$
20	Ps	Load the summator with the address part of this command	20k	—	—	$(c)=(k)$. k is a signed 12 bit number in the address field of the instruction. $k\leq 3777$.
21	E1	Conditional transfer of control	21a	Retained from the preceeding cycle	—	When $\omega=1$ the control is transferred to the command (a). When $\omega=0$ the control is transferred to the command which follows 21a.
22	E2	Unconditional transfer of control	22a	Retained from the preceeding cycle	—	The control is transferred to the command (a).
23	E3	Transfer of control according to the Key k	23k	Retained from the preceeding cycle	—	The command which follows 23k is used or not according to the position of the kth key on the console. k ranges from 1 to 7.
24	E4	Transfer of control in a cycle	24a	—	—	The control is transferred to command (a) while a cycle of commands is being repeated. After the number of repetitions is complete, the control advances to the following command in sequence. Used together with command 25n.

[2] The absence of the overflow indication in multiplication verifies that the machine represents numbers as fractions.

System of Commands for the Machine URAL-I (*Continued*)

Number of Operations	Designation of Operations	Operation	Command (base −8)	Conditions for generation of the signals		Brief description of the operation
				$\omega=1$	$\phi=1$	
25	Nts	The beginning of a cycle	25*n*	—	—	The group of commands beginning with (*a*) and ending with the command 24*a* is repeated: 1) $n+1$ times if the address is modified by one unit (*i.e.*, cycling through a sequence of half-word locations); 2) $n/2+1$ times if the address is modified by two units (*i.e.*, cycling through a sequence of full word locations). n is ≤ 3777 and is the difference between the largest and smallest addresses which can appear in any command whose address can be changed. A sign 0 with n implies half word sequencing; a sign 1, full word sequencing.
26	Sm	Accumulation of numbers $(c_0)+(a)$	26*a*	—	Blocked	$(c)=(c_0)+(a)$ with end-around carry operation.
30	Iz	Modification of command 30*a*	30*a*	Retained from the previous cycle	— —	The complement (inverse code) of 30*a* is added to the command which follows command 30*a*.
31 01 00	Lp a_1 1*c* a_2	Read numbers from a perforated tape to storage cells (a_1) through (a_2)	—	—	—[3]	Transfers the contents of the zone *c* on the perforated tape into the cells a_1 through a_2.
31 02 00	Lm a_1 2c a_2	Read numbers from a magnetic tape to storage cells a_1 through a_2	31a_1 02*c* 00a_2	—	—	Transfers contents of zone *c* of the magnetic tape into full word cells a_1 through a_2.
31 03 00	Lm a_1 3*c* a_2	Write numbers from all (a_1) through (a_2) onto the magnetic tape	31a_1 03*c* 00a_2	—	—	Recording contents of the consecutive cells a_1 through a_2 into zone *c* of the magnetic tape; a_1 and a_2 must be full word addresses.
32	Pch	Printing the number (c_0)	34 0000	—	—	Printing (c_0) in the octal or decimal system depending upon the position of the key "Print" on the control panel. When the key "Perforation" on the printing device is "on," (c_0) is punched on the punched tape of the output perforator in either binary or binary coded decimal.
34	In	Advance paper	34 0000	—	—	The paper of the printing device advances for one line without printing.
37	Os	Stopping of machine	37*a*	—	—	Stopping of machine with the lighting of indicator *a* on console.

[3] The three type-31 instructions require supplementary information in the following two half words. They are shown as a triad of instructions. Although not elsewhere defined, the operation code 00 appears to be the "no operation" instruction. In these instructions, there is the restriction that binary information can be placed in either full or half word locations, but binary-coded-decimal information must be placed in a full word cell.

Appendix II

URAL-II Instruction Repertoire

The following information about the instruction repertoire of URAL-II was obtained at the Penza factory. It is not complete and is in somewhat different form than the table for URAL-I. However, an effort has been made to resolve the uncertainties and to complete the description of each instruction. It appears that, as indicated, several instructions of URAL-II are the same as URAL-I. The Russian idiom has not been replaced by English idiom except where necessary to clarify meaning.

List of Commands of the Machine URAL-II

Notation: (*a*) Contents of cell *a* in ferrite store

Number	Name of Command	Designation of Command	Operation Code (Base 8)	Time of Execution of Command (Microsec.)		Notes
				With Full Words (40 Bits)	With Half Words (20 Bits)	
1	Addition with a floating point	Slp(*a*)	41	150 (average)	—	

List of Commands of the Machine URAL-II (*Continued*)

m-er	Name of Command	Designation of Command	Operation Code (Base 8)	Time of Execution of Command (Microsec.)		Notes
				With Full Words (40 Bits)	With Half Words (20 Bits)	
2	Addition with a fixed point	Slf(a)	01	80	80	
3	Subtraction with a floating point	Vchp(a)	43	150 (average)	—	
4	Subtraction with a fixed point	Vchf(a)	03	80	80	
5	Subtraction of moduli with a floating point	Vchm(a)	44	150 (average)	—	
6	Multiplication with a floating point	Ump(a)	46	490 (maximum)	—	
7	Multiplication with a fixed point	Umf(a)	06	470	330	
8	Division with a floating point	Dlp(a)	47	830 (maximum)	—	
9	Division with a fixed point	Dlf(a)	07	810	470	
10	Set sign	Fz(a)[1]	10	80	80	
11	Logical shift	Se(k)	11	130+10k	130+10k	The direction of shift depends on the sign of k which is in the address field.
12	Arithmetic shift	Sd(k)	11	130+10k	130+10k	If there is an indication of a full word in the command, the shift is logical; if not, it is arithmetic.
13	Extraction of part of the number	Vd(a)[1]	12	80	80	
14	Formation (of number)	Fr(a)[1]	13	80	80	
15	Comparison (of numbers)	Sr(a)[1]	14	80	80	
16	Loading the summator with floating point information	Psp(a)	42	85	—	
17	Loading the summator with fixed point information	Psf(a)[1]	02	80	80	
18	Loading the summator from t th input	Ps(t)	40	80	80	(t is the number of input.)
19	Loading an accumulator[2] with floating point information	Pnp(a)	56	170	—	
20	Loading an accumulator[2] with fixed point information	Pnf(a)	16	160	160	
21	Transfer of control first	El(a)[1]	21	80	80	If $\omega=1$,[3] and there is not an indication of a full word, the control is transferred to the command in cell a.
22	Transfer of control first	El(a)[1]	21	80	80	Control is transferred to the command in cell a if $\omega=0$ and there is an indication of a full word in the command.
23	Transfer of control second	E2(a)[1]	23	80	80	Control is always transferred to cell a.
24	Transfer of control third	E3(k)[1]	23	80	80	Depending upon the position of the kth key, the command following E3k is, or is not, fulfilled.

[1] This command appears to be the same as the URAL-I command which has the same operation code.

[2] This command is almost certainly a "store summator in ferrite store" operation. This is deduced from the similarity of the operation de (16) of instruction 20 to the operation code (16) of URAL-I's store command (number 16). "Accumulator" must therefore refer to a store cell in the ferrite store.

[3] There is no information about the indicating signal ω. Presumably, it behaves much like the corresponding signal in URAL-I.

List of Commands of the Machine Ural-II (*Continued*)

Number	Name of Command	Designation of Command	Operation Code (Base 8)	Time of Execution of Command (Microsec.)		Notes
				With Full Words (40 Bits)	With Half Words (20 Bits)	
25	Transfer of control fourth	E4(a)[1]	24	80	80	To be used after a group of commands whic are executed repeatedly with the help of com mand Nts(p).
26	Beginning of the cycle	Nts(p)[1]	25	80	80	The command Ntsp in conjunction with com mand E4a makes it possible to execute repea edly a group of commands and to change th addresses of commands having the applicab tag.
27	Load the accumulator with the counter of cycles	Pnts(a)[4]	27	160	—	
28	Change of command	Iz(a)[1]	30	80	—	The contents of cell a are added to the conten of the command register before executing th command following this command.
29	Summation	Sm(a)[1]	26	80	—	The command is used for obtaining contr sums.
30	Printing of the result in a decimal system	Pchd(t)	32	20 numbers/sec.	—	t is the number of the printing (output) d vice.
31	Printing of the result in the octal system	Pchv(t)	33	20 numbers/sec.	—	t is the number of the printing (output) d vice.
32	Skip or space a line	In(t)[1]	34	20 lines/sec.	—	t is the number of the printing (output) devic
33	Block transfer[5] to punched tape	Lp(a_1)[6] (C) (a_2)	50	150 numbers/sec.		
34	Block transfer to a magnetic drum for reading	Mbch(a_1)[6] (a_3) (a_2)	51	5000 numbers/sec.	—	
35	Block transfer to a magnetic drum for reading without writing unto the ferrite accumulator[7]	Mlch(a_1)[6] (C) (a_2)	54	1000 numbers/sec.	—	An indication of a full cell is placed at addre a_1.
36	Block transfer to magnetic drum for writing	Mbz(a_1)[6] (a_3) (a_2)	52	5000 numbers/sec.	—	
37	Block transfer to magnetic tape for reading	Mlch(a_1)[6] (C) (a_2)	53	1000 numbers/sec.	—	
38	Block transfer to magnetic tape for reading without writing on ferrite accumulator[7]	Mlch(a_1)[6] (C) (a_2)	53	1000 numbers/sec.	—	An indication of a full cell is placed at addre a_1.
39	Block transfer to magnetic tape for writing	Mlz(a_1)[6] (C) (a_2)	54	1000 numbers/sec.	—	
40	Halt	0c	37	—	—	

[4] This command almost certainly stores the contents of some special counter in the ferrite store. This counter evidently is associated wit the cyclic repetition of a group of commands. This repeating loop probably utilizes commands 26 and 27 in the same way as URAL-I.

[5] The Russian word used here (обращение) implies the notion of "return to." It seems best translated here as "block transfer."

[6] The details of these seven instructions are not known. However, by comparing the various rates and reasoning in terms of similar opera tions in URAL-I, it appears that they may operate as follows:

a) Number 33 is the block transfer from cell a_1 through cell a_2 of the ferrite store into zone C of the perforated tape.
b) Number 34 is the block transfer to cell a_1 through cell a_2 of the ferrite store from the magnetic drum, starting with cell a_3 of the drun
c) Number 35 is the block transfer to zone C of the magnetic tape from cell a_1 through cell a_2 of the magnetic drum. This is a direct trans fer not involving the ferrite store.
d) Number 36 is the block transfer from cell a_1 through cell a_2 of the ferrite store to the drum, starting at cell a_3 of the drum.
e) Number 37 is the block transfer to cell a_1 through cell a_2 of the ferrite from zone C of the magnetic tape.
f) Number 38 is the block transfer from cell a_1 through cell a_2 of the magnetic drum into zone C of the magnetic tape. This is a direc transfer not involving the ferrite store.
g) Number 39 is the block transfer from cell a_1 through cell a_2 of the ferrite store into zone C of the magnetic tape.

The structure of URAL-II, however, permits a multiplicity of magnetic tapes and drums. It may be, therefore, that a_3 is the addres of a particular drum and C, the address of a particular tape unit. If so, it isn't clear how the first location on the drum or the zone on th tape is specified. It is clear, however, from a comparison of the operating rates that there is a direct drum-tape and tape-drum transfer.

[7] Here, again, "accumulator" must refer to a storage cell in the ferrite store.

Appendix III

Evaluation of Soviet Union Ferrite Square-Loop Cores[38]

The seven samples of USSR ferrite cores include th memory cores and switch cores. Sample types were follows:

1) BT-1 (1958),[39] OD = 0.080 inch, ID = 0.050 inch ×1.3 mm). This core has a pulse coercivity of approxiately 1.35 oersteds.

The BT-1 cores (same size) received in 1959 were und to be equivalent to those received in 1958 with e exception that the uniformity of the most recent res is greater. The pulse characteristics of this core e plotted in Figs. 60 and 61. All plots are the average five cores tested. Disturbed "one" output dV_1, disrbed "zero" output dV_z, switch time t_s, and peaking me t_p, are plotted as functions of drive. The pulse proam is shown in Fig. 62.

The disturb ratio of I_K/I_R is the ratio of the threshold rrent I_k (the drive which disturbs a core from its manent flux state) to the switching drive I_R. This sturbed ratio measures the degree of nonlinearity assoated with minor loop operation of the core.

These cores have a signal-to-noise ratio which apears acceptable for small size coincident current memies (below 4096 words). The disturb ratio (I_K/I_R) is mparable to the present state of the core art in the nited States. It is, however, coupled with a rounded nee, which may be a result of adding zinc to the comosition. This is done at the expense of a deteriorated gnal-to-noise ratio and Curie point. Adding zinc to oth switch and matrix cores has been the trend for the ast several years, because it results in an improved witching constant.

The switching constant (Fig. 63) is 1.4 oersted-μsec hich compares with 0.8 to 1 oersted-μsec for the present tate of the art in the United States.

This core is representative of the early state of the nemory core art in the United States. It could be used n a medium size (below 5000 words) 15–20-μsec coincient current memory or an 8-μsec word-organized memry.

The physical and electrical uniformity of the more ecent BT-1's is better than those received in 1958 but is elow present production standards in this country.

2) BT-1 (1959), OD = 0.050 inch, ID = 0.030 inch 1.40×0.8 mm). Fig. 61 is a plot of BT-1 material made nto a 50-mil OD core. The characteristics indicate that t is the same material as the 80-mil BT-1 sample. The ore has a reasonable signal-to-noise ratio but the disurb ratio at suggested drive (475 ma) is 0.615. This is elatively poor by the presently accepted standard which exceeds 0.65).

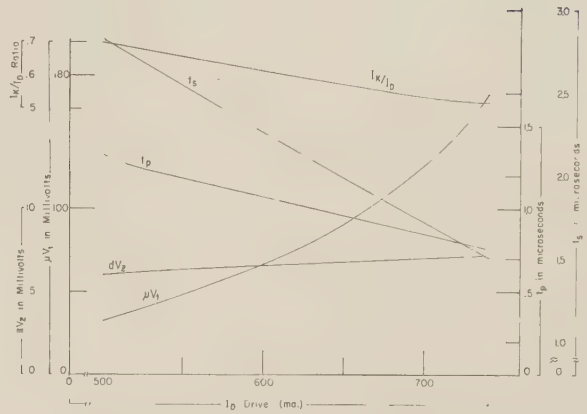


Fig. 60—BT-1 characteristics: 2×1.3 (1958).

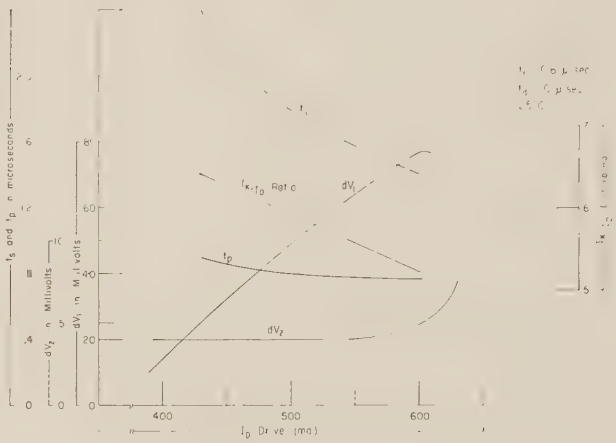


Fig. 61—BT-1 characteristics: 1.4×0.8 mm (1959).

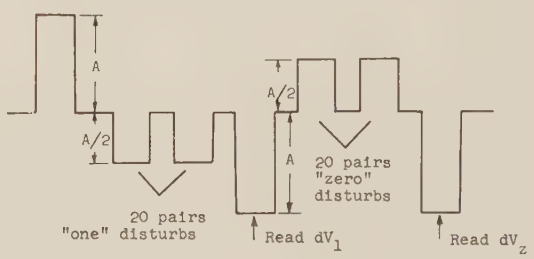


Fig. 62—Program of test pulses.

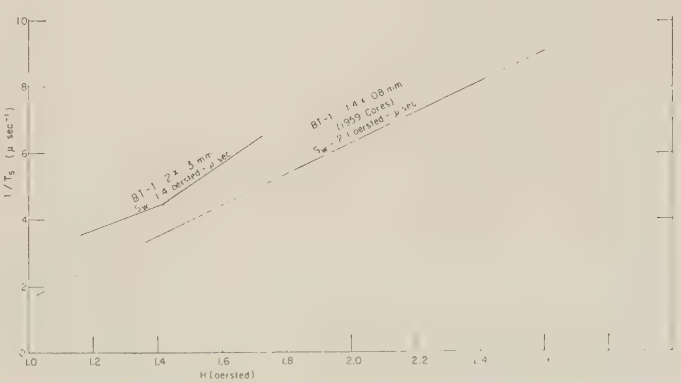


Fig. 63—BT-1 switching constants.

[38] This section is based on a report prepared by Telemeter Magetics Corporation under a subcontract with The RAND Corporaon.

[39] This sample was received by the Scott, *et al.*, party.

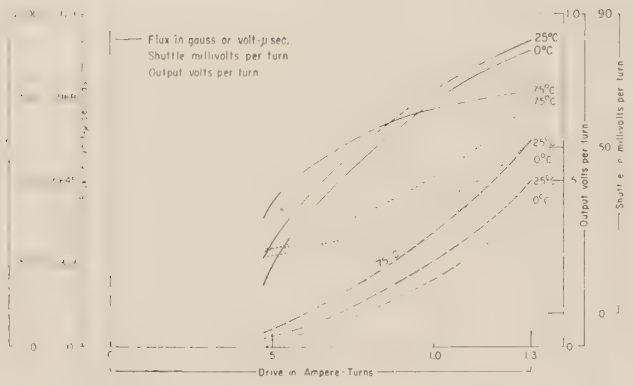


Fig. 64—BT-2 characteristics: 3×2 (1958).

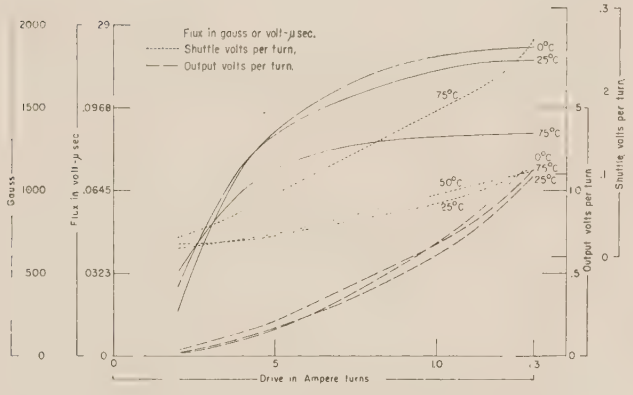


Fig. 65—BT-5 characteristics: 3×2 (1959).

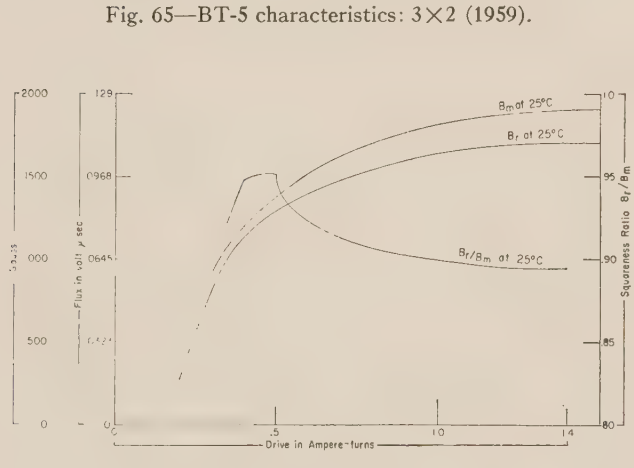


Fig. 66—BT-5 characteristics: 3×2 (1959).

The switching constant for this core (Fig. 63) is quite poor, 2.1 oersted-μsec. This deterioration may be due to serious deviation in pressing density. These cores are definitely inferior to the 80-mil BT-1 cores. They are representative of early laboratory samples made in this country during the transition from 80- to 50-mil cores.

3) K-28 (1959), OD=0.120 inch, ID=0.080 inch (3×2 mm). This is very similar to the BT-1 material. It has a pulse coercivity of approximately 1.6 oersteds. Operated in a coincident current memory, this core would require 1 ampere-turn full drive and could operate with a 15–20-μsec cycle time. It has a good disturb ratio coupled with a rounded knee which results in a relatively poor signal-to-noise ratio. In a "word-select" store, this core could operate with approximately an 8-μsec cycle time (min.).

All other cores received of this dimension (3×2 mm) are switch cores. Normal application as a memory element for a core of this size would be for buffer or logic applications where multi-turn windings are desired but the array size is limited to several thousand bits.

4) BT-2, OD=0.120 inch, ID=0.080 inch (3×2 mm). This sample is by present United States standards a high drive switch core. Fig. 64 is a plot of the shuttle volts, volts per turn, and flux at three different temperatures. All readings were taken under pulse conditions with a 10-μsec pulse width, 0.3-μsec pulse rise time. The pulse coercivity calculated from Fig. 64 is 0.97 oersteds.

BT-2 cores have a higher Curie temperature than BT-5 (270°C vs 150°C) with a resultant higher coercivity. They also have better shuttle characteristics than BT-5. Where this is a serious consideration such as in a large switch application, BT-2 would be used in preference to BT-5.

5) BT-5. This 3×2 mm core is considered a low drive core by United States standards. Fig. 65 is a plot of the same characteristics as discussed with regard to BT-2. Fig. 66 is a plot of the squareness ratio and ϕ vs drive characteristics. The pulse coercivity calculated from Fig. 66 is 0.485 oersteds.

The BT-2 and BT-5 cores are quite representative of the present state of the switch core art in the United States. Detailed analysis shows small differences between BT-5 and equivalent United States cores.

While the ferrite switch core technology of the Soviet Union is roughly on a par with that of the United States, this is not true, however, of the memory core art. For example, the BT-1 core is representative of the early "S-2" cores which are now considered obsolete. The drive requirements are roughly twice that required by United States cores for equivalent output and switching times.

Curves which are representative of production memory cores in the United States are included in Figs. 67–69. The size of these cores is roughly equal to the Soviet cores and, therefore, they can be compared directly. Fig. 70 is a glossary of relevant terminology.

Chemical Composition of Soviet Cores

The chemical composition of the cores has been determined by emission spectroscopy (Fig. 71). Such analyses are ordinarily accurate to approximately ±30 per cent of the amount of each element present. This precision is completely satisfactory for the minor constituents, but is somewhat lacking in the case of the major constituents. Nonetheless, if this type of information is combined with nonstructure sensitive magnetic properties, such as Curie temperature and saturation magnetization, and if similar spectrochemical analyses of cores for which more accurate knowledge of the gross

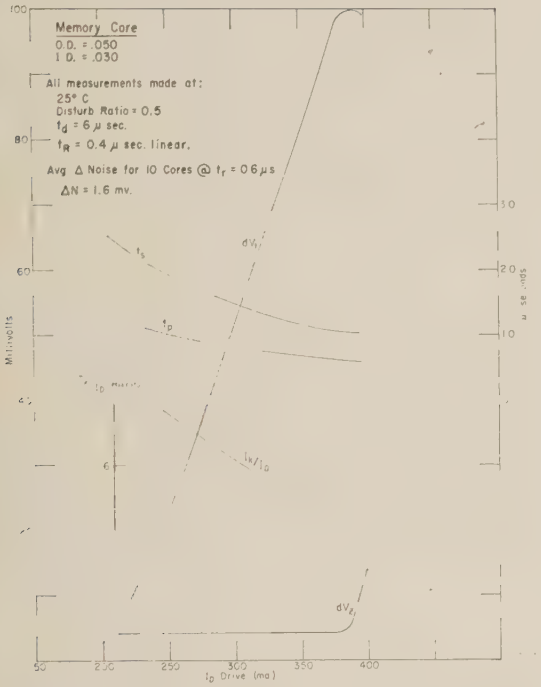


Fig. 67—Typical U. S. memory core characteristics.

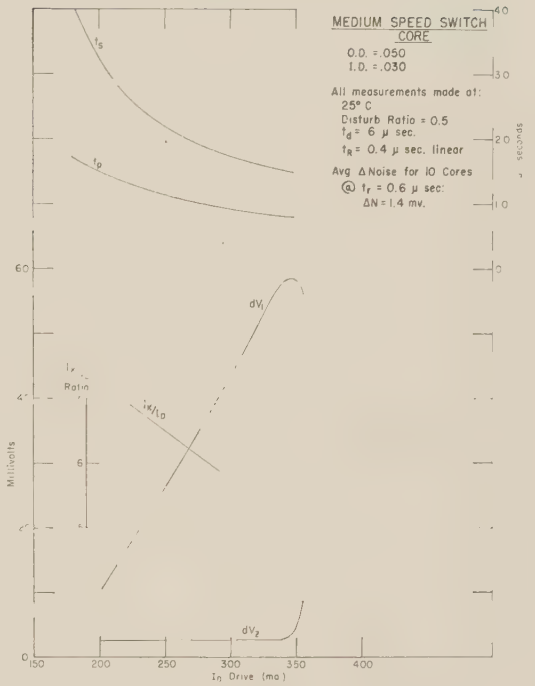


Fig. 68—Typical U. S. switch core characteristics.

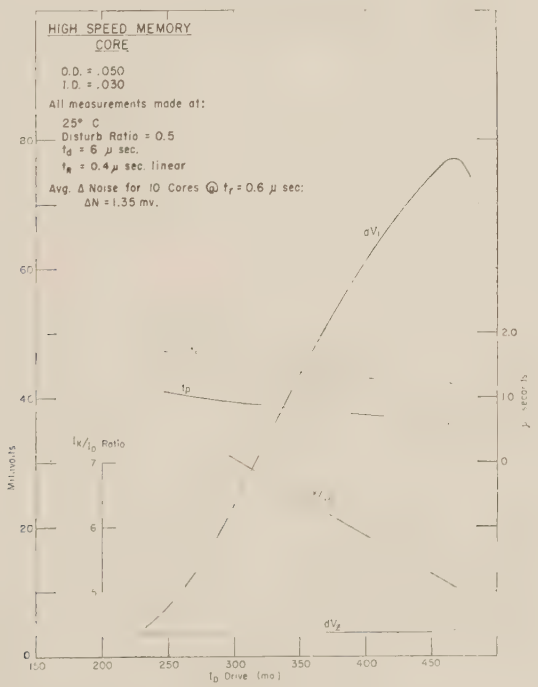


Fig. 69—Typical U. S. switch core characteristics.

I = amplitude of current pulse at time t_p;
t_0 = reference time, designated as 10 per cent of I on the rise of a read pulse;
t_r = rise time of current pulse from 10 per cent to 90 per cent of I;
t_w = width of current pulse from 90 per cent to 90 per cent of I;
t_d = duration of current pulse from t_0 to 90 per cent of the fall time of I;
t_f = fall time of the current pulse from 90 per cent to 10 per cent of I;
uV_1 = the undisturbed "selected-one" voltage of a core;
dV_1 = the disturbed "selected-one" voltage of a core;
dV_2 = the disturbed "selected-zero" voltage of a core which has been disturbed only by partial write pulses;
t_p = peaking time of the "one" voltage of a core measured from t_0;
t_s = switching time of a core measured from t_0 to the point where the dV_1 signal has decreased to 10 per cent of its peak value;
I_r = the read current pulse;
B_r = remanent flux density;
B_m = saturation flux density;
Shuttle Voltage = output from a non-reset switch core.

Fig. 70—Glossary of magnetic core notation.

	Material			
	BT-1 Per cent	BT-2 Per cent	BT-5 Per cent	K-28 Per cent
Iron	61.0	60.0	57.0	54.0
Manganese	5.8	7.2	6.2	12.6
Zinc	1.1	nil	4.3	0.19
Calcium	0.092	0.60	1.1	0.046
Magnesium	2.3	2.5	1.7	3.2
Silicon	0.012	0.0097	0.014	0.015
Copper	0.016	0.019	0.014	0.016
Nickel	0.010	0.016	0.0055	0.0069
Cobalt	0.0079	0.0088	0.0074	0.0077
Aluminum	0.0051	trace	0.0079	trace
Chromium	0.0018	0.0033	0.0020	0.0024
Other elements	nil	nil	nil	nil

All data ±30 per cent

Fig. 71—Chemical composition of Soviet cores.

chemical composition is known, the composition of unknown cores can be related rather closely to known cores.

As far as the minor constituents (silicon, aluminum, chromium, copper, nickel, and cobalt), are concerned, the Soviet cores are all as pure as representative U. S. cores. This may indicate good sources of high purity raw materials. It may also indicate small scale laboratory production, which is usually easier to control than large scale manufacture.

Calcium, which is now considered a deleterious impurity, is present to about 0.7 per cent in type BT-5 and 0.6 per cent in BT-2. At an early date it was mistakenly thought that calcium has some virtues and was present, for example, in early "S-1" cores. U. S. Patent No. 2,715,109 of 1955 relates to the use of calcium in producing square loop ferrites. No U. S. manufacturer now includes calcium in a square loop ferrite mix.

The major constituents of Soviet cores are oxides of magnesium, manganese, zinc, and iron. As in the American cores, zinc oxide is substituted in order to decrease coercivity and lower the Curie temperature. Samples K-28 and BT-2 had no zinc, but the zinc content increases fourfold from BT-1 to BT-5. Corresponding Curie temperatures are: BT-1, $T_c = 280°C$; BT-2, $T_c = 270°$; and BT-5, $T_c = 150°$.

The iron content of the Soviet cores is undoubtedly similar to that used in U. S. cores since saturation flux densities are similar in both. (Saturation flux density decreases sharply with decreasing iron content.)

The ratio of magnesium to manganese is the most difficult parameter to assess, since there is a 2:1 spread in the data. However, the ratio of magnesium to manganese in all of the Soviet cores seems to be considerably lower than what is found in contemporary U. S. cores

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Composite List of Publications Received as a Result of the USA-USSR Cultural Exchange April–May 1959

(Most publications are in Russian; a few, in English or French)

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[4]	Problems in Cybernetics, Vol. 1—Moscow, 1958; 268 pp.[1,2]	A. A. Liapunova, Ed.	Physico-Mathematical Literature Publications

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[40] Digital Computer Basic Units Using Junction Transistor Elements of Pulse-Potential Type—Moscow, 1958; 35 pp.[2] Yu. I. Sharapov

[41] Some Principles of Designing Magnetic Permanent Storage Devices—Moscow, 1957; 37 pp.[2] Yu. I. Vizun

[42] Experiments with automatic translation on the electronic calculating-machine BESM—Moscow, 1956; 28 pp.[2] I. S. Mukhin

[43] Experiments with automatic translation on the electronic calculating-machine BESM—Priroda, August, 1956.[2] G. P. Zelenkevich, N. L. Korolev, S. N. Razoumovskiy

[44] Accelerating Multiplication and Division in High Speed Digital Computers—Moscow, 1958; 25 pp.[2] V. S. Burtsev

	Title	*Author*	*Source*
[45]	Concerning the Problem of Machine Translation of Languages—Moscow, 1956; 35 pp.[2]	D. Panov	USSR Academy of Sciences
[46]	Questions of Computer Mathematics and Techniques (Articles) Third Edition—Kiev, 1958; 98 pp.[2]		Academy of Sciences
[47]	Les Experiences de Traduction Automatique de l'Anglais en Russe a l'Aide de la Calculatrice BESM.[2]	N. L. Korolev S. N. Razoumovskiy G. P. Zelenkevitch	International Congress on Cybernetique—Nemur, 1956
[48]	Les Chiffres de Base du Developpement de l'Economie Nationals de l'U.R.S.S. pour 1959–1965. Theses du Rapport du Camarade N. Khrouchtchev au XXI[e] Congres du P.C.U.S., Moscow, 1958.[1]	N. S. Khruschchev	Unknown

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Correspondence

Analog-Computer Representation of Inelastic Stops*

Analog-computer representation of stops and barriers must involve a simulation of the actual forces exerted by the stop upon the impinging mass.[1,2] An *inelastic stop* at $X \geq X_1$ is correctly represented by a force which reduces the simulated velocity dX/dt to zero quickly as soon as X exceeds X_1 (see Fig. 1).

The only correct relay-circuit representation of an inelastic stop known to the writer was given by Johnson,[1] who did not, however, label his stop as "inelastic." Fig. 2 shows an up-to-date equivalent of Johnson's circuit. The input voltage F represents a force which drives a mass into the stop at $X \geq X_1$. F is integrated twice to yield voltages $-dX/dt$ and X, respectively, representing velocity and displacement.

Fig. 1.

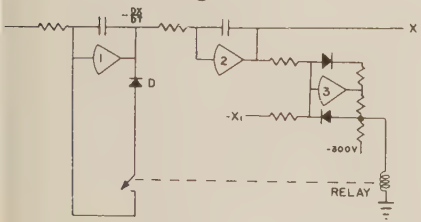

Fig. 2.

The block on the right is a comparator circuit which actuates the relay when X exceeds X_1, causing the relay contact to close. The resulting short circuit across the integrating capacitor of integrator 1 is equivalent to a large viscous force proportional and opposite to the velocity (represented by dX/dt) with which the mass attempts to penetrate the barrier. Because of the "anti-stick" diode D, the viscous force acts only when $dX/dt > 0$. Hence the mass will not stick to the stop when the applied force F is reversed (one would otherwise simulate a stop coated with chewing gum).

For faster computations it is desirable to do away with relay circuits and their inherent time delays.

To the best of the writer's knowledge, no accurate diode representation of an inelastic stop has been published; the approximate diode representations given previously[2] do not discharge the integrating capacitor correctly.

Fig. 3 shows a new diode circuit for the purpose. When X exceeds X_1 the comparator output voltage E changes abruptly from zero to about -60 volts and turns the diode switch made up of diodes D_1 and D_2. The circuit acts just like the relay circuit; note that no "anti-stick" diode is needed, since the switch passes current in one direction only. Fig. 4 shows a typical record of X and $-dX/dt$ vs time obtained with constant positive F. A similar reversed diode switch can be added across the first switch in the case of particles constrained to move between two inelastic stops at X_1 and X_2.

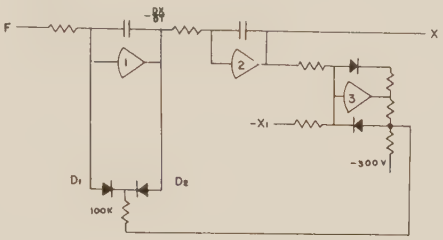

Fig. 3.

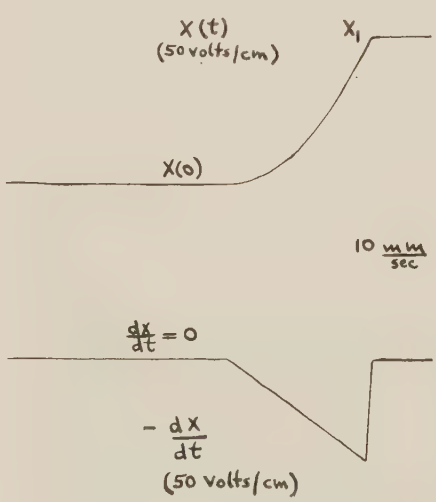

Fig. 4.

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Analysis and Methods for Detection of Some DC Amplifier Errors*

Tests which permit an operator to check his analog computing equipment in place are of great value, and an effort is being made to increase the amount of information that may be obtained in this manner. The purpose of this correspondence is to show the effects of summing-junction grid current and to outline a method for detecting it. A method for checking the dc gain of the chopper amplifier is included. It is felt that these tests should be used as weekly machine checks.

Fig. 1 shows a simplified block diagram for the dc amplifier when used as an inverter.

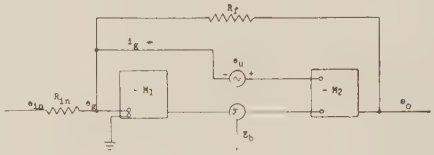

Fig. 1.

The output voltage may be written as shown in

$$e_0 = -M_2[(1 + M_1)e_g + e_u - E_b] \quad (1)$$

where

M_1 = gain of chopper amplifier.
M_2 = gain of main dc amplifier.
e_u = an unbalance voltage resulting from variations in power supplies, filament supplies, and input tube characteristics.
E_b = balance voltage introduced by balance pot.

Summing the currents at the e_g node and solving for e_g gives

$$e_g = \frac{R_f R_{in}}{R_f + R_{in}}\left[-i_g + \frac{e_{in}}{R_{in}} + \frac{e_0}{R_f}\right]. \quad (2)$$

Substituting (2) into (1), and solving for the output voltage gives

$$e_0 = -\left[\frac{M_2(R_f + R_{in})}{R_f + R_{in}[1 + M_2(1 + M_1)]}\right] \cdot \left[\frac{R_f R_{in}(1 + M_1)}{R_f + R_{in}}\left(\frac{e_{in}}{R_{in}} - i_g\right) + e_u - E_b\right]. \quad (3)$$

Since we are interested mainly in the dc value, and at dc $M_1 \gg 1$ and $M_2 \gg 1$, (3) can be simplified to

$$e_0 \approx -R_f\left(\frac{e_{in}}{R_{in}} - i_g\right) - \left(\frac{R_f + R_{in}}{R_{in}M_1}\right)(e_u - E_b). \quad (4)$$

The importance of low grid current is obvious from this equation (the effect of the i_g term is greatly increased in an integrator) and a value of approximately 10^{-4} μa has been set as the maximum allowable. It also indicates that the grid current could be balanced out by adjusting E_b. This solution is impractical, however, in that the balance would have to be obtained for a particular set of input connections, and any modification of the inputs would necessitate rebal-

* Received by the PGEC, October 13, 1959.
[1] C. L. Johnson, "Analog Computer Techniques," McGraw-Hill Book Co., Inc., New York, N. Y.; 1956.
[2] G. A. Korn and T. M. Korn, "Electronic Analog Computers," McGraw-Hill Book Co., Inc., New York, N. Y., 2nd ed.; 1956.

* Received by the PGEC, September 24, 1959

ancing. We can take advantage of this property for detecting grid current, since the other sources of an unbalance voltage (e_u are affected by the same factor as E_b.

To take a more quantitative look at this, assume the input to be grounded ($E_{in}=0$) and the amplifier balanced ($e_0=0$), then (4) reduces to:

$$E_u - E_b = \frac{R_f R_{in_1} M_1}{R_f + R_{in_1}} I_g. \tag{5}$$

Then replace R_{in_1} with R_{in_2} in (4) (with e_1 still grounded), and substitute (5) for $e_u - E_b$ and solve for i_g which gives

$$I_g = \frac{R_{in_2}(R_f + R_{in_1})}{R_f^2(R_{in_2} - R_{in_1})} E_0. \tag{6}$$

In practice, R_f would be the normal 1-meg feedback resistor, and R_{in_1} and R_{in_2} could be 1-meg and 100-K input resistors. A highly damped microvolt meter should be substituted for the panel meter in order to detect grid currents of the level of interest. Using these resistors and the procedure indicated, a grid current of 10^{-4} μa would produce an output of -0.45 millivolts. Repeating the procedure with R_{in_1} and R_{in_2} reversed would give an output of 82 microvolts per 10^{-4} μa of grid current.

In the case of the integrator, R_f was replaced by $1/c_f s$ in (3) and the equation was solved for I_g in a similar manner. The approximate solution for the range of t of interest is

$$I_g = \frac{R_{in_2} c_f}{R_{in_2} - R_{in_1}} \frac{e_0}{t}. \tag{6a}$$

For the case where R_{in_1} and R_{in_2} have the values given above and $c_f=1$ microfarad. e_0 drifts at the rate of -54 millivolts per minute per 10^{-4} μa of grid current. Reversing R_{in_1} and R_{in_2} and repeating the procedure would give a drift rate of 5.4 millivolts per minute per 10^{-4} μa.

To obtain the approximate gain of the chopper balance amplifier, we return to (4) and note the sensitivity of e_0 with respect to E_b:

$$\frac{de_0}{dE_b} = -\frac{R_f + R_{in}}{R_{in} M_1} \tag{7}$$

or

$$M_1 = \frac{R_f + R_{in}}{R_{in}} \frac{\Delta E_b}{\Delta e_0}. \tag{8}$$

A measure of M_1 may then be obtained by varying the balance pot from end to end, noting the swing of the amplifier output, and substituting values into (8). Because of loading, the absolute value of M_1 obtained from the equation may be greatly in error for a certain type amplifier. However, in checking a large number of identical amplifiers of this type, relative gain of the chopper amplifiers may be obtained with this method, and marginal or low gain amplifiers detected.

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Minimization of Contact Networks Subject to Reliability Specifications*

Introduction

The purpose of this paper is to extend the Quine-McCluskey method of minimizing contact networks,[1-3] to cases where the contacts are susceptible to erroneous operation.[4] The networks discussed are of the "and-to-or" type, where each series path is the realization of a different "one" transmission in the given contact function. The failures considered are those which occur when one or more contacts remain permanently open. Under these conditions it may be desired to synthesize networks which will remain operative despite the failure of a specified number of contacts. This number will be called the "reliability level" of the synthesized network. In the following sections a procedure will be discussed for constructing minimal networks consistent with a specified reliability level.

The Prime Implicant Matrix

The first step in the procedure is the determination of all the prime implicants associated with the contact function to be realized. This can be done by the Quine-McCluskey method to yield a set of Boolean terms, each of which implies at least one transmission in the function. Synthesizing a network such that each path will correspond to a different prime implicant is certain to realize the given function. If each path is repeated $r+1$ times, the result is a realization with the reliability level r.

To minimize the described network, it is advantageous to construct the "prime implicant matrix," where the columns correspond to the prime implicants, and the rows to the specified transmissions. The element common to row X and column Y is unity if the transmission X is implied by the prime implicant Y, and is zero otherwise. If the synthesized network is to have the reliability level r, each prime implicant should be represented in the matrix by $r+1$ identical columns. As an example, matrix (1) is a prime implicant matrix constructed for the transmissions whose decimal equivalents are 0, 2, 7, 8, 9, 13 and 15, with the reliability level 1. The six prime implicants are designated by A, B, C, D, E and F. The significance of the additional column on the right, called the "indicator column," will become apparent later.

$$\begin{array}{c} \\ 0 \\ 2 \\ 7 \\ 8 \\ 9 \\ 13 \\ 15 \end{array} \begin{array}{c} \begin{array}{cccccccccccc} A & A & B & B & C & C & D & D & E & E & F & F \end{array} \\ \left[\begin{array}{cccccccccccc} 1 & 1 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 & 1 & 1 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 1 & 1 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 & 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 & 1 & 1 \end{array}\right] \end{array} \begin{array}{c} \\ 2 \\ 2 \\ 2 \\ 2 \\ 2 \\ 2 \\ 2 \end{array} \tag{1}$$

* Received by the PGEC, August 4, 1959; revised manuscript received, October 30, 1959. The research reported here was supported by the U. S. Navy under contract with the University of California, Berkeley.

[1] W. V. Quine, "A way to simplify truth functions," *Am. Math. Monthly*, vol. 62, pp. 627–631; November, 1955.

[2] E. J. McCluskey, Jr., "Minimization of Boolean functions," *Bell Sys. Tech. J.*, vol. 35, pp. 1417–1444; November, 1956.

[3] S. H. Caldwell, "Switching Circuits and Logical Design," John Wiley and Sons, Inc., New York, N. Y., ch. 5; 1958.

[4] E. F. Moore and C. E. Shannon, "Reliable circuits using less reliable relays," *J. Franklin Inst.*, vol. 262, pp. 191–208, 281–297; 1956.

To minimize a contact network with a reliability level r, it is necessary to find the smallest set of prime implicants, such that each transmission would be implied at least $r+1$ times. In terms of the prime implicant matrix, this corresponds to deleting the largest number of columns such that each row would contain at least $r+1$ unities. This problem is identical with that encountered in minimal-scan pattern recognition under noisy conditions, discussed in detail elsewhere.[5] The procedure for minimizing the prime implicant matrix will be presented, therefore, without a proof.

A Minimization Procedure

1) Construct the prime implicant matrix for the prescribed contact function and reliability level r, and call it the "first-order matrix set." Let all the elements in the indicator column of this matrix be $r+1$. Let k be an index with an initial value 1.

2) On each matrix in the kth-order matrix set, carry out the following operations: a) Locate any row with the least number of unities. b) Produce new matrices by deleting, one at a time, columns in which the located row is unity. c) Produce the indicator column of each new matrix by subtracting, term by term, the deleted column from the indicator column of the originating matrix.

3) From any group of identical matrices constructed in 2) eliminate all but one. Call the remaining matrices the "$(k+1)$th-order matrix set."

4) Test whether any indicator column in the $(k+1)$th-order set consists entirely of zeros. a) If such a column exists, the columns which are absent from the corresponding matrix represent the minimal set of prime implicants. b) If such a column does not exist, delete from each matrix in the set all rows which have a zero in the indicator column. Add 1 to k and return to 2).

As an example, the following matrices represent the 9th-order matrix set produced by applying the proposed procedure to the prime implicant matrix (1):

$$\begin{array}{c} \\ 9 \\ 13 \end{array} \begin{array}{c} \begin{array}{cccc} D & D & F & F \end{array} \\ \left[\begin{array}{cccc} 1 & 1 & 0 & 0 \\ 1 & 1 & 1 & 1 \end{array}\right] \end{array} \begin{array}{c} \\ 0 \\ 2 \end{array} \qquad \begin{array}{c} \\ 9 \\ 13 \end{array} \begin{array}{c} \begin{array}{cccc} C & D & F & F \end{array} \\ \left[\begin{array}{cccc} 1 & 1 & 0 & 0 \\ 0 & 1 & 1 & 1 \end{array}\right] \end{array} \begin{array}{c} \\ 0 \\ 1 \end{array}$$

$$\begin{array}{c} \\ 9 \\ 13 \end{array} \begin{array}{c} \begin{array}{cccc} C & C & F & F \end{array} \\ \left[\begin{array}{cccc} 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 \end{array}\right] \end{array} \begin{array}{c} \\ 0 \\ 0 \end{array} \qquad \begin{array}{c} \\ 13 \end{array} \begin{array}{c} \begin{array}{cccc} B & D & F & F \end{array} \\ \left[\begin{array}{cccc} 0 & 1 & 1 & 1 \end{array}\right] \end{array} \begin{array}{c} \\ 1 \end{array}$$

$$\begin{array}{c} \\ 13 \end{array} \begin{array}{c} \begin{array}{cccc} B & D & D & F \end{array} \\ \left[\begin{array}{cccc} 0 & 1 & 1 & 1 \end{array}\right] \end{array} \begin{array}{c} \\ 1 \end{array} \qquad \begin{array}{c} \\ 13 \end{array} \begin{array}{c} \begin{array}{cccc} B & C & F & F \end{array} \\ \left[\begin{array}{cccc} 0 & 1 & 1 & 1 \end{array}\right] \end{array} \begin{array}{c} \\ 0 \end{array}$$

$$\begin{array}{c} \\ 13 \end{array} \begin{array}{c} \begin{array}{cccc} B & C & D & F \end{array} \\ \left[\begin{array}{cccc} 0 & 1 & 1 & 1 \end{array}\right] \end{array} \begin{array}{c} \\ 0 \end{array} \qquad \begin{array}{c} \\ 13 \end{array} \begin{array}{c} \begin{array}{cccc} B & B & F & F \end{array} \\ \left[\begin{array}{cccc} 0 & 0 & 1 & 1 \end{array}\right] \end{array} \begin{array}{c} \\ 0 \end{array}$$

$$\begin{array}{c} \\ 13 \end{array} \begin{array}{c} \begin{array}{cccc} B & B & D & F \end{array} \\ \left[\begin{array}{cccc} 0 & 0 & 1 & 1 \end{array}\right] \end{array} \begin{array}{c} \\ 0 \end{array} \qquad \begin{array}{c} \\ 13 \end{array} \begin{array}{c} \begin{array}{cccc} B & B & D & D \end{array} \\ \left[\begin{array}{cccc} 0 & 0 & 1 & 1 \end{array}\right] \end{array} \begin{array}{c} \\ 0 \end{array}$$

Applying 4) to this set yields the following combinations of prime implicants, each of which represents a possible minimal realization:

$$\begin{array}{c} AABBDDEE \\ AABCDDEE \\ AABCDEEF \\ AACCDDEE \\ AACCDEEF \\ AACCEEFF \end{array}$$

[5] A. Gill, "Minimal-scan pattern recognition," IRE Trans. on Information Theory, vol. IT-5, pp. 52–58; June, 1959.

Conclusion

A network with a reliability level r can ways be constructed by placing in parallel -1 networks of reliability level 0. The pro- dure outlined above, however, is prefera- e inasmuch as it yields all possible minimal mbinations of prime implicants; some mbinations may be more desirable than hers, due to the difference in the number contacts involved in the various impli- nts.

The minimization procedure, which is tlined in the form of a computer program, indeed suitable for automatic execution a general-purpose digital computer. This ature is especially useful when the given ntact function has too many variables to minimized by inspection, by trial-and- ror, or by semisystematic means currently use.

Finally, by putting $r=0$, the proposed rocedure can be adapted to problems where liability is immaterial. In this form, the rocedure becomes an ordinary prime im- icant minimization scheme, to supplement her schemes already described in the erature.

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Two Modulator-Switches for Com- uter Applications*

Electromechanical relay tree selection evices that are used with a serial drum emory are necessarily slow and it was in- nded to replace these by an all-electronic witching system. A voltage switch for the urpose of reproducing and a current switch or that of recording signals was designed for ach channel of the drum. Four voltage witches with a common post-amplifier and our current switches with a common cath- de (feed) modulating input are shown in igs. 1 and 2, respectively. These were tried ith a serial magnetic drum storage memory aving a clock pulse repetition frequency of 0 kc and which had each of its read-write eads with two separate windings, the re- istance of each winding being 0.8 ohm. The stimated signal voltage when reproducing as about 5 mv while the signal current re- uired for recording purposes was of the rder of 0.5 ampere rms. A control apparatus, escribed elsewhere,[1] generates selector volt- ges (+100 volts when selected and +70 olts when not selected) at the terminals of a elector switch that is meant for selecting ne of the many read-write heads. With the elp of the same control apparatus, a se- uence of 32 bits (a word) can be recorded n or reproduced from any of the four chan- els, each channel of the drum having 16

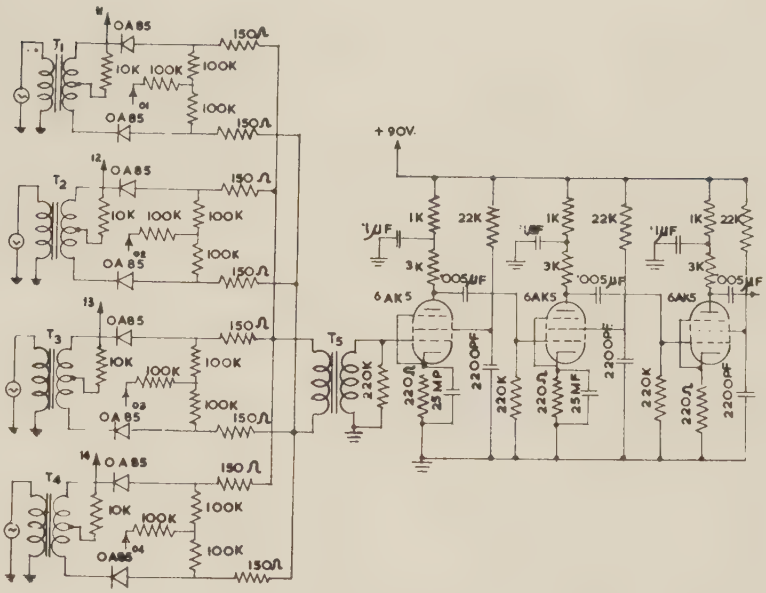


Fig. 1—Four voltage switches with a common post-amplifier for reproducing signals from a magnetic drum memory.

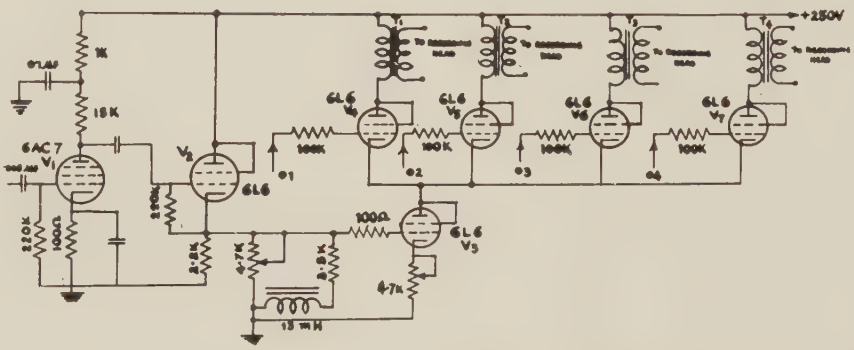
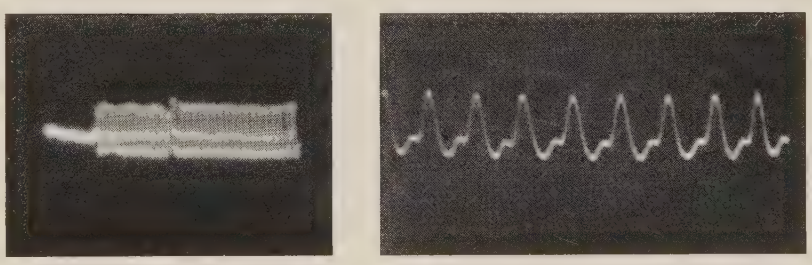


Fig. 2—Four current switches with common input (source) meant for recording signals on a magnetic drum.



(a) (b)

Fig. 3—(a) 32 bits of a word recorded and reproduced with the aid of the switches in Figs. 2 and 1, respectively; (b) signals in (a) in more detail.

words. Whenever a word is recorded (or reproduced) from the drum an "operation complete" pulse is generated. This pulse is used to change 1) the address and 2) the code of operation. In the present case, the operations were only of two kinds, "read" or "write." The code of the address can be changed 1) by selecting any one of the four channels and 2) by selecting any one of the 16 words on the channel. The channel address was always changed either to 0, 1, 2, or 3 and the word address by 1 only. This meant that the switches were tested for selecting and for reproducing or recording any two (neighboring) consecutive words which happened to be on different channels. Fig. 3(a) shows the oscillogram of a word that was recorded and later reproduced in this fashion with the aid of above shown switches. Fig. 3(b) shows in more detail a portion of a complete word. For the drum memory used in these experiments, two consecutive words on a channel have a free interval of 200 μsec, but the switches are capable of realizing switching times of the order of only a few μsec; this and other points are discussed in brief in the following.

* Received by the PGEC, June 18, 1959; revised manuscript received November 12, 1959.

[1] D. S. Kamat, "Control apparatus for a serial drum memory," *Electronic Engrg.*, vol. 30, pp. 634–39; November, 1958

The Voltage Switch

In the case of the voltage switch (Fig. 1), a steady dc voltage equal to +80 volts is always applied at terminals 11, 12, 13 and 14, while the selector switch voltage step +70 to +100 volts will appear at one of the four terminals 01, 02, 03 or 04. Under such conditions only one pair of diodes will conduct in the forward direction while the other 3 pairs will not. The read signal voltage (e_s), selected at one head position, and the unwanted signal (e_n), appearing at the other 3 head positions, will appear together on the primary side of the transformer T_5 as the output voltage (e_0). Let the diode resistances forward and back be referred to as R_f and R_b respectively, the three 100-kΩ resistances be designated by R_1, the 10-kΩ resistance by R_3, and the 150-ohm resistance by r. Then

$$e_0 = 3e_n \frac{(R_f + r + R_3)(r + 2R_1)}{(R_3 + R_b + r)(4r + 2R_1 + 3R_f)} + e_s \frac{(R_f + R_3 + r)(r + 2R_1)}{(R_f + R_3 + r)(4r + 2R_1 + 3R_f)}. \quad (1)$$

Thus at the output terminal for values of the circuit parameters shown in Fig. 1, and for $R_b = 4$ mΩ and $R_f = 1$ kΩ, e_s and e_n appear in the proportion

$$\frac{e_s}{e_n} = \frac{3(R_b + r + R_3)}{(R_f + r + R_3)} \doteq 1000. \quad (2)$$

This value, equivalent to 60 db, represents the degree of usefulness of the modulator switch in accepting the selected signal e_s and in rejecting the unwanted signal e_n.

One has also to consider the impedance (z_0) across which e_0 appears in order to design transformer T_5 suitably. This is given by

$$z_0 = \frac{(r + 2R_1)(r + R_f + R_3)}{(4r + 2R_1 + 3R_f)} \doteq \frac{1}{3}\left[\frac{2R_1(R_f + R_3)}{2R_1 + 3(R_f + R_3)}\right]. \quad (3)$$

Also the impedance which is presented to the modulating or selector switch step voltage is given by the expression below when $R_b \gg 2R_1$:

$$\frac{2R_1}{3} + R_f + R_3. \quad (4)$$

This voltage switch has no special provision for counteracting variations in performance (*i.e.*, equalizing gains) that arise due to differences in circuit elements like diodes, except that resistance R_3 (10 kΩ), being much larger than R_f (diode forward resistance), reduces the effects due to variations in R_f [see (2)].

The other components of this switch are the step-up transformers T_1 to T_4. Each half of the secondaries of these transformers behaves as an inductor for the selector switch step voltage input. Here the design requirements are dictated by the need to establish quickly the final modulated (carrier) current. For an inductance of 100 mh and for a series resistance given by (4), 90 per cent of the final steady-state current will be established in 4 μsec. Also, the two halves of each secondary must be perfectly balanced if there is to be no interaction between the selector switch step voltage and input (read) signal source. The step-up ratio for the transformers designed is 1:25 and the core material used is the ribbon type 5000G soft magnetic alloy.

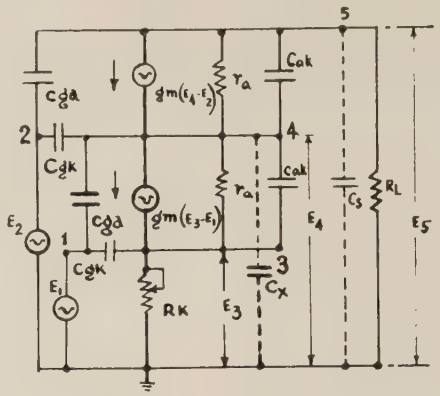


Fig. 4—Equivalent circuit of a single current switch shown in Fig. 2.

grid of V_3. Fig. 4 is an equivalent circuit fo triode V_3 and, for example, V_4 (the one tha is selected). Assuming $E_2(t)$ is a unit step voltage (corresponding to selector switch input), and after writing equations for the nodes and substituting for $C_{gk} = C_{ak} = 11$ pf, $C_{ga} = 0.04$ pf, $R_k = 1.0$ kΩ, $R_L = 0.8$ kΩ, $gm = 4.8$ ma/v, $r_a = 1.7$ kΩ, we have

$$E_5(s) = \frac{s^3 0.6847 + s^2 1.050 \times 10^8 + s 0.760 \times 10^{16} - 0.6895 \times 10^{24}}{s(s^3 + s^2 5.138 \times 10^8 + s 10.86 \times 10^{16} + 10.47 \times 10^{24})}. \quad (5$$

The Current Switch

The method of operation of this modulator switch (Fig. 2) will be such as to apply first the selector switch step voltage (+70 to +100 volts) to one of the four terminals, 01 to 04, and then to apply the input signal (32-bit word) at the grid of tube V_3. As shown in Fig. 2, the signal appears across the transformer in the anode circuit of the upper triode, the recording head winding being connected across the secondary of this transformer. The choice of the resistance (R_k) in the cathode of V_3 is determined by the requirement that the common cathode of V_4 to V_7 should be at a sufficiently high voltage level to make the three nonselected tubes remain completely cut off while the selected one, whose grid is at +100 volts, conducts. For 6L6 tubes (triode connection), a dc supply of +250 volts and selector switch step voltage of +70 to +100 volts, R_k equal to 1.0 kΩ, would result in a cathode level of +115 volts. Besides this, R_k must also be chosen so that, for the load of 0.8 Ω (resistance of the head winding) and a ±30-volt swing on the grid of V_3, a signal current of 0.5 ampere rms or more should be generated. Actually, for the transformer chosen with a step-down ratio of 30:1, the current change in the anode circuit will be about 17 ma.

Apart from the design for the requisite output signal current, the other two factors to be considered are minimizing transients that would inevitably appear across the load due to selector switch voltage input at 01, 02, etc., and designing a suitable amplification system for pulsed signal inputs at the

After finding the roots of the polynomial and taking the inverse Laplace transform of above, we have the output voltage across load as

$$E_5(+) = -0.0658 + 0.4569e^{-2.564\times10^8 t} + 0.9658e^{-1.322\times10^8 t} \cdot \cos(69° - 1.55 \times 10^8 t). \quad (6)$$

Similarly, we can obtain response characteristics for inputs at node 1, *i.e.*, for signals at grid of V_3 (in Fig. 2). This is

$$E_5(+) = -0.585 + 0.02674e^{-2.525\times10^8 t} + 1.298e^{-1.139\times10^8 t} \cdot \cos(122° - 1.657 \times 10^8 t). \quad (7)$$

Assuming an incremental voltage of +20 volts for $E_2(t)$ we can see from (6) that an incremental current of 1.50 ma would appear across the load due to the selector step voltage. From (7) it can be seen that for an input of ±30 volts at grid of V_3, the current across the load would be about 21 ma. This leads us to conclude that the unnecessary transient current due to the selector switch voltage is about 23 db below the signal strength required for recording purposes on the drum. Also, the current switch, because of the cathode regeneration, is capable of reducing variations that arise due to differences in transconductance of the switching tubes.

The author is indebted to K. M. Patnaik for his assistance in the work reported here.

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Indian Statistical Institute
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ncerning Abstracts*

An abstract is a wonderful way to tell a der whether he will be interested in an icle or whether he should pass it by. An stract should stand by itself and should ntain the complete idea of the article, or at st enough so that the reader will have few ubts as to just what is to be found in the rint should he obtain one. This imposes her severe constraints on its form and kes abstract writing, especially the writ- of a *short* abstract, quite limited in free- m.

A few authors in the TRANSACTIONS ite introductions and call them abstracts. ould the abstract be published in a place mote from the main text this can disturb the reader. The use of the future tense, especially the future promise "also treated will be the case . . . " can be unnerving to him. When he finishes the paragraph he thumbs the page frantically looking for the promised treatment. Finding none he may conclude that he lacked insight enough to find it and thus avoid that subject or that author in the future.

Conclusions are essential to an abstract. "It was found that . . . " pins things down. Here, unlike in detective novels, giving away the plot does not spoil it for the reader. The reader should wonder, perhaps, about the details of how the result was obtained, but never should he be allowed to wonder what results were obtained. What leads to the conclusion is of secondary importance to the conclusion itself. "By considering . . . " is a usable form here. The use of much more runs the danger of giving the reader a lecture rather than the abstract he wants.

The reader then expects two things in an abstract. First, a brief statement of the result, and second, a brief statement of the method. These statements might even be reduced to clauses of the same sentence. Accepting literary form rather than newspaper form, the result usually follows the remarks concerning the method.

Abstract: By considering the information desired by the reader, it was found that an abstract should contain a statement of the result and a statement of the method.

E. J. GAUSS
Numerical Analysis Research
University of California
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* Received by the PGEC, December 10, 1959.

Contributors

Samuel N. Alexander (A'44–M'55–F'55–F'56) was born in Wharton, Texas, February 22, 1910. He received both the A.B. degree in physics and the B.S. degree in electrical engineering in 1931 from the University of Oklahoma, Norman, and was awarded a Tau Beta Pi Fellowship for graduate study. In 1933 he received the M.S. degree in electrical engineering from the Massachusetts Institute of Technology, Cambridge, where he continued his graduate studies under a Coffin Foundation Research Fellowship in 1934.

N. ALEXANDER

His professional experience includes work from 1935 to 1939 as a laboratory engineer at Simplex Wire and Cable Company, and as a research assistant at M.I.T. during 1939–1940. From 1940 to 1943 he was a physicist with the Navy Department on electronic instrumentation. He became senior project engineer with Bendix Aviation Corporation on development of military telemetering equipment in 1943, and in 1946 was appointed Chief, Electronic Computers Laboratory, National Bureau of Standards, on development of digital computer technology and over-all supervisor of design and construction of SEAC and DYSEAC. From 1954 to the present he has been Chief, Data Processing Systems Division, National Bureau of Standards. This activity includes the application of digital techniques to data processing and information storage and retrieval, and the application of combined analog and digital techniques to automatic instrumentation and dynamic control systems.

Mr. Alexander is a member of Phi Beta Kappa, Sigma Xi, Tau Beta Pi, Sigma Tau, and the Washington Academy of Sciences, and was a recipient of a silver medal from the Royal Academy of Engineering Science, Stockholm, Sweden, in 1956.

❖

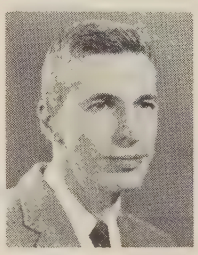
Paul Armer (M'57) was born in Montebello, Calif., on November 8, 1924. He graduated from the University of California at Los Angeles in 1946, and after spending several months with United Air Lines joined the Rand Corporation in 1947. He assumed his present position as head of the Computer Sciences Department in 1952.

P. ARMER

Mr. Armer has been active in computer professional societies and was instrumental in the formation of several cooperative computer user groups. One of these, SHARE (the IBM-704/709/7090 users cooperative), held its organizational meeting at Rand, and Mr. Armer was a member of its Executive Board during its first three years. He is also a member of the National Council of the Association for Computing Machinery and was, until the end of 1959, Vice-Chairman of the National Joint Computer Committee.

Mr. Armer is a member of the Association for Computing Machinery and AAAS.

Douglas B. Armstrong was born on March 17, 1918, in Toronto, Ontario, and received the B.A. degree from the University of Toronto in 1940. He later studied at the Massachusetts Institute of Technology, Cambridge, where he received the M.S. degree in 1951 and the Sc.D. in 1955.



D. B. ARMSTRONG

Dr. Armstrong was associated with the Canadian Marconi Company, from 1945 to 1948. In 1954 he joined the technical staff of Bell Telephone Laboratories, Murray Hill, N. J., where he has since been engaged in research in switching problems, which have included simulation and economic studies of telephone systems, studies of central office systems and reliability studies of digital systems.

Dr. Armstrong is a member of Sigma Xi.

❖

Morton M. Astrahan (S'45–A'50–M'51–SM'57), for a biography and photograph, please see page 500 of the December, 1959, issue of these TRANSACTIONS.

❖

Glenn C. Bacon was born on August 24, 1935, in Phoenix, Ariz. He received the B.S. degree in electrical engineering from the University of California, Berkeley in 1957

and is currently completing work for the M.S. degree at Stanford University, Stanford, Calif.

G. C. Bacon

He joined the IBM Research Laboratory at San Jose, Calif., in June, 1957, as an associate engineer. His initial assignment was in the area of magnetic recording head design for large-scale memories. He is presently concerned with problems in the area of the detection of signals in magnetic recording readback.

Mr. Bacon is a member of Eta Kappa Nu and Tau Beta Pi, and is an associate member of Sigma Xi.

❖

Lipman Bers was born May 22, 1914, in Latvia. He was educated in Europe, and his final degree was that of Dr. Res. Nat. from the University of Prague in 1938. His first post in America was as research associate at Brown University, Providence, R. I., from 1941 to 1945. He was assistant professor of mathematics, 1945–1948, and associate professor, 1948–1951, at Syracuse University, Syracuse, N. Y. In the academic years 1949–1951 he was a member of the Institute for Advanced Study at Princeton University, Princeton, N. J.

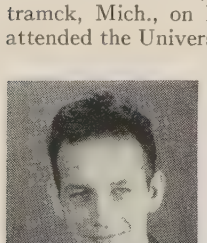
L. Bers

He became a member of the faculty of New York University in 1951 as visiting professor of mathematics, became a professor in 1953, and chairman of the Graduate School Department of Mathematics in 1959. He has received Guggenheim and Fulbright scholarships for the year 1960, and is at present on leave from New York University.

Dr. Bers has written technical papers in many journals of mathematics and applied mathematics. He is the author of the book "Mathematical Aspects of Subsonic and Transonic Gas Dynamics."

❖

Ted W. Berwin (A'55) was born in Hamtramck, Mich., on February 14, 1928. He attended the University of Detroit, Detroit, Mich., the University of Southern California, Los Angeles, and the University of California at Los Angeles. He received the B.S. degree from U.C.L.A. in 1951 and is presently a graduate student there studying mathematics, computers, closed-loop systems, and transistor electronics.

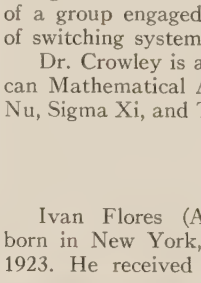


T. W. Berwin

He worked at Collins Radio Co., Cedar Rapids, Iowa, for two years on development of a narrow-band synchronous diversity radio teletype system. In 1953, he joined Rocketdyne, Division of North American Aviation, Canoga Park, Calif., for four years working on research, design and development of special instrumentation systems for rocket engine measurements. In 1957 he joined Dresser Dynamics, Northridge, Calif., and continued to work on special instrumentation systems, such as a flying spot analog-to-digital converter, data acquisition systems, engine instrumentation systems, high speed pressure and flowrate measurements, high speed cameras, and associated electronic equipment.

❖

Thomas H. Crowley (S'50–A'51–M'56) was born on June 7, 1924, in Bowling Green, Ohio. He attended Ohio State University where he received the B.E.E. degree in 1948 and the Ph.D. degree in 1954, shortly before joining the technical staff of Bell Telephone Laboratories, Murray Hill, N. J. Dr. Crowley has been engaged in studies of switching systems problems, including application of magnetic devices to switching circuits and studies of time-varying networks for time-division switching. He worked on the design of an analog-to-digital encoder. He is presently in charge of a group engaged in theoretical analysis of switching systems problems.

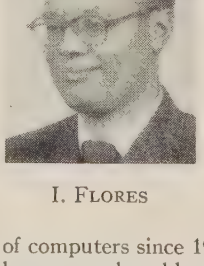


T. H. Crowley

Dr. Crowley is a member of the American Mathematical Association, Eta Kappa Nu, Sigma Xi, and Tau Beta Pi.

❖

Ivan Flores (A'51–M'54–SM'58) was born in New York, N. Y., on January 3, 1923. He received the B.A. degree from Brooklyn College, New York, N. Y., in 1948 and the M.A. degree from Columbia University, New York, N. Y., both in mathematics. In 1955 he received the Ph.D. degree in the field of supervision in industry from New York University.



I. Flores

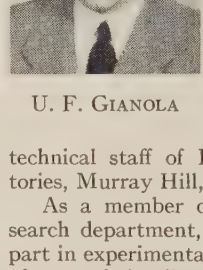
He has been working in the field of computers since 1950. From 1950 to 1953 he was employed by Mergenthaler Linotype Company, Brooklyn, N. Y., where he developed circuits for the automatic electronic justification of typographical copy. From 1953 to 1955 at Balco Labs of Newark, N. J., he supervised research and development in telemetry and automatic control by digital and analog methods, and also conducted investigations in antenna design and physical chemistry. At the Nuclear Developmer Corporation of America, he was engage from 1955 to 1957, in supervising the d sign and construction of a computer f complete inventory control of the produ tion and stock of the Otis Elevator Co pany. During 1957–1959 he was with t Remington Rand Laboratories for Advance Research, South Norwalk, Conn., where has conducted research in the field of cha acter recognition for the automatic han ling and processing of printed documen and dial systems analysis for a small co puter application and design.

Dr. Flores has been with Dunlap a Associates in Stamford, Conn., since 195 He is a major contributor for several co tracts in operations research, including t application of decision-making theory military systems and the planning of a integrated weather complex. He also teach a course in digital computers at the Pol technic Institute of Brooklyn.

Dr. Flores is a member of ACM.

❖

Umberto F. Gianola (SM'59) was bo on October 29, 1927 in Birmingham, En land, and attended the University of Bi mingham where l received the B. degree in 1948 a the Ph.D. in 195 He worked with t Royal Aircraft E tablishment, Ma vern, Eng., in 19 and as a post-doctor fellow at the Un versity of Britis Columbia, Vanco ver, from 1951 to 19 before joining t technical staff of Bell Telephone Labor tories, Murray Hill, N. J., in 1953.



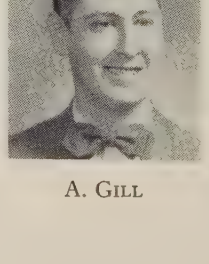
U. F. Gianola

As a member of the transmissions r search department, Dr. Gianola has take part in experimental and theoretical studi of transmission line structures, analyses of new magnetostrictive transducer, work o possible applications of solar batteries t communications channels and fundament studies of the effects of ion bombardmen More recently he has been studying solic state memory and logic devices.

Dr. Gianola is a member of the America Physical Society and the Research Societ of America.

❖

Arthur Gill was born in Haifa, Israel, o April 18, 1930. He attended the Massachu setts Institute of Technology, Cambridg Mass., where he r ceived the B.S. an M.S. degrees in elec trical engineering i 1955 and 1956, r spectively. He r ceived the Ph.D. d gree in the sam field from the Un versity of Californi Berkeley, in 1959.



A. Gill

From 1954 t 1956 he was a teach

ssistant in the Department of Electrical ineering at M.I.T. From 1956 to 1957 vorked in the research division of the rtheon Manufacturing Company, Walt-, Mass., where he was engaged primarily semiconductor circuitry design. Since he has been at the University of Cali-ia as a teaching associate in electrical neering and later as an assistant pro-or. He is also associated with the Elec-ic Research Laboratory, where he is king on information theory problems, with the advanced programming de-pment group of the Bendix Computer sion of the Bendix Aviation Corpora-.

Dr. Gill is a member of Eta Kappa Nu, Beta Pi, and Sigma Xi.

❖

Harry H. Goode (SM'52) was born on 1, 1909 in New York, N. Y. He received B.S. degree in history from New York University in 1931, the B.Ch.E. degree from Cooper Union, New York, N. Y., in 1940 and the M.A. degree in mathematics from Columbia University, New York N. Y., in 1945. He has held positions in research and development at Tufts College, Medford, Mass., at the Special De-s Center of the U. S. Navy in connection n computers and simulation, and as direc-of the Willow Run Research Center at University of Michigan in the develop-t of large-scale systems. For the last years he has taught, consulted, and ied on research in the Electrical Engi-ing Department of the University of higan.

H. H. Goode

Mr. Goode is presently Chairman of the ional Joint Computer Committee. He is ember of the Association for Computing chinery.

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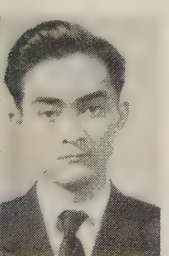
Eiichi Goto was born on January 26, 1, in Tokyo, Japan. He graduated from University of Tokyo in March, 1953, receiving the Rigakusi degree.



E. Goto

In 1954 Mr. Goto invented a subharmonic oscillator logical element called the Parametron. He built the first parametron computer, PC-1, for the University of Tokyo in 1958, and is presently engaged in the construction of the sec-l parametron computer, PC-2, for the iversity. He is also working on Esaki de circuitry. Since August, 1959, he has n an assistant professor in the Depart-nt of Physics, University of Tokyo.

He is a member of the Physical Society apan.

Louis D. Grey was born on January 20, 1928, in New York, N. Y. He received the B.S.S. degree from the College of the City of New York in 1949 and the M.S. degree in mathematics from New York University in 1956, where he is currently working for the Ph.D. degree in mathematics.

L. D. Grey

He has been a research assistant at the Institute of Mathematical Sciences at New York University and has also been an assistant engineering mathematician in the University's Engineering Research Division where he was engaged in the study of weather phenomena. He joined the Remington Rand Univac Division, South Norwalk, Conn. in 1956 and worked on the mathematics of character recognition. Since 1958, he has been employed as a mathematician by the Teleregister Corporation of Stamford, Conn., where he is currently engaged in the simulation of communication systems.

Mr. Grey is a member of the American Mathematical Society, the Mathematical Association of America, the Society for Industrial and Applied Mathematics, and the Association for Computing Machinery.

❖

Albert S. Hoagland (S'50–A'54–SM'57) was born on September 13, 1926, in Berkeley, Calif. He received the B.S. degree in 1947, the M.S. degree in 1948, and the Ph.D. degree in 1954, all in electrical engineering at the University of California, Berkeley.

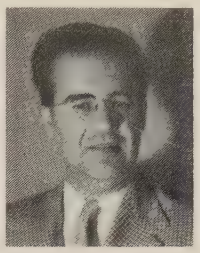
A. S. Hoagland

He was project engineer on the California Digital Computer Program, 1948 to 1950. From 1954 to 1956, he was a consultant for IBM and assistant professor at the University of California, Berkeley, teaching senior and graduate courses in switching theory and computers. He joined the staff of the IBM Research Laboratory in San Jose, Calif., in 1956, where he was a senior engineer in charge of file memory research, and is now manager of engineering sciences for the San Jose Research Laboratory. He is a registered professional engineer in the State of California.

Dr. Hoagland is a member of AIEE, Phi Beta Kappa, Sigma Xi, Eta Kappa Nu, and Tau Beta Pi.

❖

Harry D. Huskey (A'49–M'55) was born in Whittier, N. C., on January 19, 1916. He received the B.S. degree from the University of Idaho in 1937, and the M.S. and Ph.D. degrees from Ohio State University, Columbus, in 1940 and 1943, respectively. He became interested in the computer field while an instructor at the University of Pennsylvania, Philadelphia in 1943–1946, where he worked on the ENIAC project.



H. D. Huskey

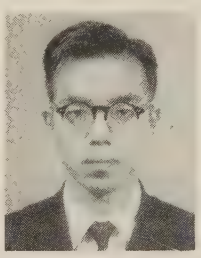
During 1947 he was in England at the National Physical Laboratory working on the ACE computer project. Subsequently he worked for the National Bureau of Standards in Washington, D. C., later transferring to a field station, the Institute for Numerical Analysis on the UCLA campus. There he was responsible for the design and construction of the National Bureau of Standards Western Automatic Computer (SWAC). In 1952–1953 he was technical director of the computation Laboratory at Wayne State University, Detroit, Mich. In 1954 he joined the faculty of the University of California at Berkeley, where he is now professor of electrical engineering and mathematics.

In the summers of 1955 and 1959 he worked on logical design and the programming of computers at the Mathematical Center, Amsterdam, The Netherlands. During the Fall term of 1959 he gave a course on computers at Cambridge University, England. He has been a consultant to the Bendix Computer Division since 1954, and worked on the logical design of the Bendix G-15 and G-20 computers.

Dr. Huskey is a member of the American Mathematical Society, ACM, and AAAS.

❖

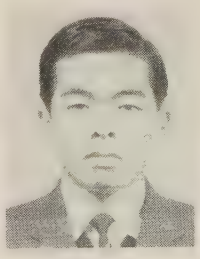
Yoshihiro Ishibashi was born in Fukuoka, Japan, on July 23, 1935. He received the Rigakushi degree in physics from the University of Tokyo in 1958. He is now a student in the postgraduate course and is engaged in the construction of the parametron computer PC-2 under the direction of Professors H. Takahashi and E. Goto.



Y. Ishibashi

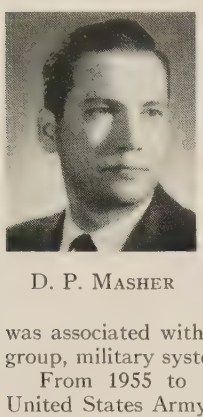
❖

Haruhisa Ishida was born in Shoka, Formosa on October 30, 1936, and received the Rigakushi degree in physics from the University of Tokyo in 1959. He is now a student in the postgraduate course and is engaged in the construction of the parametron computer PC-2 under the direction of Professors H. Takahashi and E. Goto.



H. Ishida

Dale P. Masher (M'54) was born in Bedford, Ind. on April 14, 1929. He received the A.B. degree magna cum laude from Harvard College, Cambridge, Mass. in 1951, and the M.S. degree in electrical engineering from the Massachusetts Institute of Technology, Cambridge, in 1953.



D. P. Masher

From 1953 until 1955, he was a member of the technical staff of Bell Telephone Laboratories. During this period he was associated with the computer research group, military systems department.

From 1955 to 1957 he served in the United States Army, attached to the Solid State Devices Branch of the Signal Engineering Laboratories, Fort Monmouth, N. J. He served as project engineer on numerous industrial preparedness study contracts for the development and production of switching transistors.

In 1957 he joined the staff of Stanford Research Institute, Menlo Park, Calif. His work in the Computer Techniques Laboratory has included the development of transistor logic circuits, the design of transistor-driven core storage units, and system responsibility for a special-purpose magnetic tape to magnetic tape converter.

Mr. Masher is a member of Phi Beta Kappa and Sigma Xi.

❖

Yasushi Matsu-Oka was born in Tokyo, Japan on July 7, 1929. He received the Kogakushi degree from Tohoku University, Sendai in 1953. Since that time he has been employed by the Hokushin Electric Work Corporation, Tokyo, where he was engaged in the development of a magnetic drum. Since 1959, he has been in the Faculty of Engineering, University of Tokyo, as a visiting research worker, where he is engaged in research on electronic digital computers under the direction of Professor T. Moto-Oka.

Y. Matsu-Oka

❖

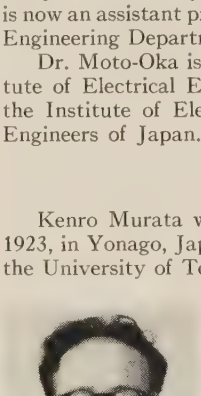
Robert McNaughton received the Ph.D. degree in philosophy from Harvard University with a dissertation in mathematical logic. He had a personal contract to do work in formal set theory from the Office of Naval Research at the Illinois Institute of Technology during 1952–1953. He taught in the Philosophy Departments of Ohio State University, and the University of Michigan (1953–1954) where he worked on a project in computing machinery sponsored by the Burroughs Corporation. He was at Stanford University from 1954 to 1957 and worked on the logical design of computing machinery under contract to the Office of Ordnance Research.

Since 1957 he has been an assistant professor at the Moore School of Electrical Engineering, University of Pennsylvania. He lectures on computers and automata, and is also engaged in switching theory projects sponsored by the Army and Air Force.

Dr. McNaughton is a member of the Council of the Association for Symbolic Logic. He was a coauthor of a paper which was awarded the Franklin Institute's Levy Medal in 1956.

❖

Tohru Moto-Oka was born in Tokyo, Japan, on April 7, 1929. He received the Kogakushi degree in electrical engineering from the University of Tokyo in 1952. From 1952 to 1957, he was a special research student at the graduate school of the University of Tokyo and engaged in research on an electronic digital computer. He received the Kogaku Hakase degree from the University of Tokyo in 1957 and joined the staff, where he is now an assistant professor in the Electrical Engineering Department.

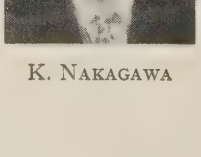


T. Moto-Oka

Dr. Moto-Oka is a member of the Institute of Electrical Engineers of Japan, and the Institute of Electrical Communication Engineers of Japan.

❖

Kenro Murata was born on October 4, 1923, in Yonago, Japan. He graduated from the University of Tokyo in 1945, receiving the Kogakushi degree. Since October, 1957, he has been a lecturer in the Faculty of Engineering, University of Tokyo, and is now engaged in the construction of the digital computer TAC at that University.

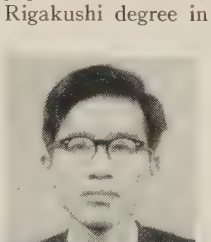


K. Murata

Mr. Murata is a member of the Mathematical Society of Japan and the Institute of Electrical Communication Engineers of Japan.

❖

Keisuke Nakagawa was born in Tokyo, Japan on March 31, 1935, and received the Rigakushi degree in physics from Waseda University, Tokyo. He is now a student in the postgraduate course and is engaged in the construction of the parametron computer PC-2 under the direction of Professors H. Takahashi and E. Goto.



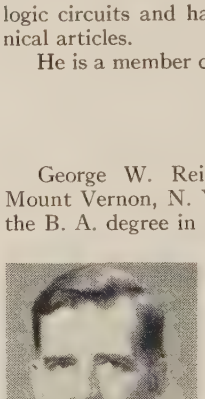
K. Nakagawa

Kisaburo Nakazawa was born on Oct ber 2, 1932, in Tokyo, Japan. He graduat from the Department of Applied Phy ics, University Tokyo, in Marc 1955, and will co plete the post grad ate course in appli physics in Marc 1960. He is present engaged in the co struction of the ele tronic digital co puter TAC at t University of Toky

K. Nakazawa

❖

Edmund E. Newhall (S'49–A'51), w born on May 26, 1927, in Calgary, Albert Canada, and received the B.S. degree in eng neering physics fro the University of A berta in 1949. He w associated with t Westinghouse Ele tric Company Rad Division, until 19 when he went to t University of T ronto, Ontario, Ca He taught electron circuits and receive the Ph.D. degree 1958, shortly befo joining the technical staff of Bell Telepho Laboratories, Murray Hill, N. J.



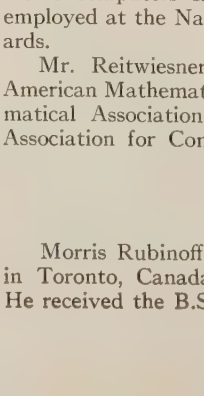
E. E. Newhall

Dr. Newhall has been engaged in r search on ferrite devices for memory an logic circuits and has written several tec nical articles.

He is a member of the AIEE.

❖

George W. Reitwiesner was born i Mount Vernon, N. Y. in 1918. He receive the B. A. degree in mathematics from Ne York University i 1939, and the S.M degree in computin from Harvard Grad uate School in 195 From 1940 to 194 he served with th Army Ordnance De partment, and fro 1947 to 1949 wa employed at the Ba listic Research Labo ratories. He ha worked with elec tronic computers since 1948, and is no employed at the National Bureau of Stand ards.



G. W. Reitwiesner

Mr. Reitwiesner is a member of th American Mathematical Society, the Mathe matical Association of America, and th Association for Computing Machinery.

❖

Morris Rubinoff (A'50–M'55) was bor in Toronto, Canada, on August 20, 191 He received the B.S., M.A., and Ph.D. de

s in physics in 1941, 1942, and 1946, ectively, from the University of Toronto. During World War II he participated in proximity fuse research at the University of Toronto and in England. In 1946 he joined the staff of Harvard University, Cambridge, Mass., as instructor in physics and Fellow in applied science at the Computation Laboratory. From 1948 to 1950 he assisted in the design he electronic digital computer at the itute for Advanced Study at Princeton versity, Princeton, N. J. In 1950 he sferred to the Moore School of Electrical ineering, University of Pennsylvania, adelphia, where he was engaged in lecng in the field of digital computers, in arch on digital real-time simulation, and elephone switching.

I. Rubinoff

n 1957 he took a leave of absence to the Philco Corporation as chief engineer computers. Among other computer activ- there, he assisted in the design of the n-high-speed transistorized computer nsac S-2000. In 1959 he returned to his of associate professor of electrical enering at the Moore School.

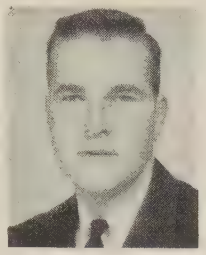
Dr. Rubinoff is a member of the AIEE, Association for Computing Machinery, Society for Industrial and Applied hematics, the American Association of versity Professors, and Sigma Xi.

❖

Takashi Soma was born in Taipei, Forsa on October 11, 1934. In 1948 he was atriated to Japan. In 1953 he entered the physics course, Faculty of Science, University of Niigata. After graduating in 1957 he entered the graduate course of physics, Department of Science, University of Tokyo. He obtained the Rigaku-shushi degree in 1959 and entered the Doctorate course. Mr. Soma is presently ened in the design of the parametron comer PC-2 under the direction of Professors Takahashi and E. Goto.

T. Soma

Sam D. Stearns was born in Seattle, Wash. on June 18, 1930. He received the B.S. degree in electrical engineering from Stanford University, Stanford, Calif., in 1953. He received the M.S. degree in electrical engineering from the University of New Mexico, Albuquerque, in 1957, and is currently working towards the doctorate.



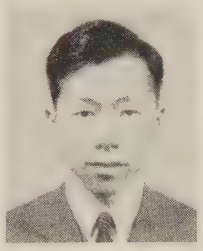
S. D. Stearns

From 1953 to 1957, he served in the U. S. Navy as a line officer aboard ship and as a physics instructor in the Armed Forces Special Weapons Project at Sandia Base, N. Mex. From 1957 to 1959, he was an engineer at Sandia Corporation in Albuquerque, where he is currently employed as a consultant to the Automated Data Development Department.

Mr. Stearns is a member of Sigma Xi, Phi Kappa Phi, Kappa Mu Epsilon, and the International Association for Cybernetics.

❖

Eiiti Wada was born in Tokyo, Japan, on June 1, 1931. He received the Rigakushi and Rigaku-shushi degrees in physics in 1955 and 1957, respectively, from the University of Tokyo. In 1955 he joined the Digital Computer Laboratory, Department of Physics, University of Tokyo, where he designed circuits for digital computers and organized the program libraries.



E. Wada

❖

Willis H. Ware (A'43–SM'49) was born in Atlantic City, N. J., on August 31, 1920. He received the B.S. degree from the University of Pennsylvania, Philadelphia, in 1941, and, as a Tau Beta Pi Fellow, the S.M. degree from Massachusetts Institute of Technology, Cambridge, in 1942.

From 1942 to 1946 he was employed by the Hazeltine Electronics Corporation for research and development in radar and IFF. In 1946 he became one of the original members of the staff of the Electronic Computer Project at the Institute for Advanced Study, Princeton, N. J. There he worked on the design and development of a large-scale general-purpose electronic digital computer, which was to set the pattern for the later construction of several other "Princeton-class machines." Simulataneously, he continued his graduate work at Princeton University, from which he received the Ph.D. degree in 1951. In 1952 Dr. Ware joined the Rand Corporation, where he is continuing his work in the applications of digital machines, as well as in research and development of high-speed computing devices.

W. H. Ware

Dr. Ware is a member of Tau Beta Pi, Sigma Xi, Eta Kappa Nu, and Pi Mu Epsilon.

❖

Hisao Yamada (A'55) was born on June 8, 1930 in Tokyo, Japan. He received the B.S.E.E. degree in 1953 from the University of Japan, where he worked on the design of an electronic computer from 1952 to 1954. He came to the United States as an exchange student in 1954, after he was awarded a Stanvac Scholarship of Japan and a Fulbright Grant, and began his studies at the Moore School of Electrical Engineering. He joined the staff as an assistant instructor in 1955, was promoted to instructor in 1957, and associate in 1959. From 1955 to 1958 he worked on logical design and traffic study for an electronic telephone system in an Army-sponsored project, receiving the M.S.E.E. degree for his thesis on this subject. He then became engaged in research for a project in general switching theory sponsored by the Air Force. Currently he is making a study of growing automata for an Army project on switching theory, and is a candidate for the Ph.D. degree with a dissertation on this subject.

Mr. Yamada is a member of the Institute of Electrical Engineers of Japan and the Institute of the Electrical Communication Engineers of Japan.

Reviews of Books and Papers in the Computer Field

EDITED BY E. J. MCCLUSKEY, JR.

Comments and suggestions on this new feature of IRE TRANSACTIONS ON ELECTRONIC COMPUTERS are solicited. Address them either to Professor McCluskey or to H. E. Tompkins, *Editor.*

The Parametron, a Digital Computing Element which Utilizes Parametric Oscillation—Eiichi Goto. (PROC. IRE, vol. 47, pp. 1304–1316; August, 1959.)

In 1954 Eiichi Goto at the University of Tokyo proposed that subharmonic oscillators could be used as the basic building block of a durable, inexpensive digital computer. Subharmonic oscillators were not new, the principle having been studied many years ago and the device utilized as a frequency divider. Dr. Goto recognized, however, that the phase ambiguity of the subharmonic signal could be used to advantage in a computer. When operating with a two-to-one division ratio, the subharmonic oscillator can have two distinct signal phases, 0° and 180°. These two phases can represent a 0 and 1 in a binary digital computer. It was also in 1954 that the late John von Neumann independently described the parametric oscillator as a means of achieving high computing speeds through the use of a microwave carrier. Unlike von Neumann's idea, which is only now being studied in American laboratories, Dr. Goto's proposal of a slower speed magnetic oscillator was pursued vigorously and has resulted in several complete computers. In fact it is claimed that nearly half of the digital computers built in Japan utilize the parametric device, now called the "Parametron."

The Parametron consists of a balanced tuned circuit utilizing either two magnetic cores or a single magnetic structure having two holes. The magnetic material is biased by a dc field to a nonlinear region on the B-H loop to achieve the variable inductance needed for parametric oscillations. Melda's experiment of exciting a mechanical resonator at frequency f by modulating the tension at 2 farads is cited as a good example of a parametric device. The mathematics of the phenomenon has been treated many times and is not repeated. Instead, a simple development of a negative conductance component due to a time varying inductance is presented. The more difficult analysis of the amplitude limiting mechanism is left for the appendix.

The operation of the Parametron is likened to a superregenerative amplifier. To control the phase of the Parametron, a quench mechanism destroys the existing information. The Parametron is then reenergized and the growing subharmonic locks in phase with the input signal. If no input signal is present, the phase is undetermined and is initiated by noise in the circuit. In the appendix a solution to the limiting nonlinear differential equation is given and the resulting integral curves are utilized in the text to show how input signals differing from 0° to 180° are restandardized to the proper phase in the Parametron. As in the more common form of a superregenerative amplifier, very large gains can be achieved in the Parametron, limited only by circuit noise. A reported gain of 100 db was mentioned. The large available gain makes possible a fan out of 10–20. A fan out of 15 was quoted for the commercially available Parametrons.

If the Parametron is operated in a detuned condition, then a mode referred to as "hard" oscillation occurs as opposed to the normal "soft" oscillation. In this state, oscillations at the subharmonic will not grow from noise or a small locking signal but require a much larger input signal of proper phase to initiate oscillation. Since this mode has the three possibilities of no oscillation, 0° phase oscillation and 180° phase oscillation such Parametrons are termed "tristable" or "ternary." Other papers[1] on parametric oscillators have shown that a detuned oscillator will have a tristable state at low excitation levels and a bistable mode at higher excitation levels, presumably due to a shift in tuning as the excitation swings further into the nonlinear region of the variable parameter being utilized. Goto does not mention any uses of this mode of operation.

[1] L. S. Onyshkevych, W. F. Kosonocky, and A. W. Lo, "Parametric phase-locked oscillator—characteristics and applications to digital systems," IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-8, pp. 277–286; September, 1959.

The appendix shows the need for a damping component in t oscillating circuit to insure cessation of the subharmonic signal wh the exciting source is periodically removed by the clock. Yet if t damping is too large, the superregenerative gain mechanism will lost. The optimum damping value for the Parametron has been fou by experiment.

The limiting mechanism is derived as a detuning of the circuit d to the nonlinear variation of the inductance. An increasing loss mec anism might also be expected but it is claimed that the detuni mechanism is sufficient to account for the limiting action observ experimentally.

The Parametron is utilized as a majority logic element, not d similar to resistive matrix logic utilizing a threshold device such as tube or transistor. The primary difference is that with a carrier sy tem two phases may cancel, thus permitting simple majority log functions. With any odd number of inputs one phase will predomina and the Parametron will lock and amplify that phase. It appears th at the present state of development, 5 inputs are the maximum nur ber that can be utilized reliably and most of the circuits shown r quired only three inputs. Together with the NOT function which simply achieved by an inverting transformer, the majority logic e ment suffices for all logical operations. Examples of a flip-flop, binary counter, a binary full adder, and a parity-check circuit a given. It is shown that the logic operations AND and OR are sp cial cases of majority logic where one of three or two of five inpu are biased by signals representing 0 or 1, respectively.

Dynamic computer circuits generally require a clock and t Parametron computer is no exception. It requires clocking for a reas even more basic than timing. Once the Parametron is oscillating, e ergy travels bidirectionally from it, feeding back into the input well as into the output. It is shown how a two-phase clock system w not suffice unless some unidirectional element is used in the inp lines. A three-phase clock system achieves the necessary unidire tional information flow and is utilized in all of the Parametron co puters. Each Parametron is quenched for approximately half t clock period and is active for the other half. Of the three clock phas the two successive phases overlap so as to couple signal informati in the proper direction through the computer. The maximum usab clock frequency is related to how rapidly the Parametron can quenched and reactivated. Of the Parametron computers cited, o of the largest (9600 Parametrons) and fastest, employed a 100- clock together with a 6-mc exciting frequency. The upper clock fr quency claimed for the Parametron itself was 150 kc. If this pertai to the period of one of the phases, the effective computing spe could be roughly three times this or 450 kc. Though Goto admits th may seem unfavorable when compared to the potentialities of tra sistors, it is not too unfavorable when compared to commercial co puters in present use. Indeed, the parametric device utilizing i proved magnetic materials or variable capacity elements holds pro ise of exceeding the computing speed of all presently known devic

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RCA Laborator
Princeton, N.

Microwave Parametric Subharmonic Oscillators For Digital Co puting—Fred Sterzer. (PROC. IRE, vol. 47, pp. 1317–1324; Augus 1959.)

Sterzer describes several clever microwave circuits useful in digit applications. The principles of operation for amplification, scali and various logic operations are given, accompanied by experiment verification that with these circuits, digital rates in excess of 100 m

be achieved with present *S*-band components. The emphasis is ed on individual circuits rather than a complete set of circuits principles for the design of a computer or data processing system. hese methods are primarily based on the subharmonic oscillator D) approach using the phase of an alternating current signal as nformation bearing parameter, an approach which has received n publicity recently.[1] However, elements of amplitude script nes[2] are employed also, and the important task of conversion be- n amplitude and phase scripts is shown to be elementary.

he chief contributions of the author are the many uses he demon- es for planar transmission line hybrid rings and the ways he uses modulation to control the presence, absence, or time of onset of lation in the SHO's. The hybrid ring is a passive element that be used together with threshold detectors to perform AND, OR Exclusive-OR functions and alone to allow script conversion and terialization of information flow. Since it is a wavelength deter- d structure, its size, at *S* band, is large for use in a complex sys- However, this improves with an increase in the microwave fre- cy employed. Bias modulation is important as a way of convert- base-band pulse information into microwave form—a must in the n of practical microwave digital systems. Moreover, the author oses that it is superior in speed to the usual scheme of pump ulation that is normally described for causing information to from one element to another. However, the major interest in microwaves is to achieve higher speeds than obtainable by l base-band methods, and including base-band pulses throughout a machine seems to be partially defeating the purpose.

nother novel technique that the author introduces is forced hing of SHO's with gain in which a control signal smaller in nitude than the output of the SHO can force the SHO to change e. To cause the required change in loading of the oscillator, a stant power" source for the controlling signal is necessary. Al- gh not mentioned by the author, this is necessary to insure that ffective loading on the oscillator varies as desired.

he circuits and techniques described by the author are valuable ibutions to the store of knowledge now building up on how to rm digital operations with microwaves.

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Springfield, Va.

large number of papers treating this subject in detail have been published ly by several authors including Billings, Blattner, Enomoto, Gold, Goto, g, Hilibrand, Kosonocky, Lo, Mueller, Muroga, Onyshkevych, Oshimo, Pohm, r, Stocker, Takoshima, von Neumann, Watanabe, Wigington, and others. Representative papers in this field are: W. C. G. Ortel, "Nanosecond logic by tude modulation at *X*-band," IRE Trans. on Electronic Computers, vol. pp. 265–271, September, 1959; and W. Sauter and P. J. Isaacs, "Microwave circuits using diodes," IRE Trans. on Electronic Computers, vol. EC-8, 02–307, September, 1959.

um Valves in Pulse Technique—P. A. Neeteson. (The Macmillan pany, New York, N. Y., second edition, 1959. 190 pp.)

his relatively short British book has more of the characteristics monograph on certain basic types of multivibrator circuits than general textbook on pulse circuits using vacuum tubes. The sec- edition differs from the first primarily by the addition of a 24- chapter on blocking-oscillator circuits.

he vacuum tube is considered as being equivalent to a switch n subjected to large amplitude signals, and a detailed, but rather entary, discussion is given to its characteristics as a switching ent. An idealized linear equivalent circuit is used in the region in h the tube exhibits gain. The transients in these circuits are yzed by using the principle of superposition and adding equiva- voltage or current functions to represent the effects of closing or ing switches at various points within the circuit. This procedure ther cumbersome and the author illustrates it by drawing dia- s, which he incorrectly calls equivalent circuits, incorporating voltage and current generators. An elementary survey of Heavi- s operational calculus is also included, although, in the reviewer's ion, the use of the Laplace transform method of solving linear rential equations would have been preferable.

ollowing this discussion of large-signal transients in electron circuits, the major part of the book is devoted to an analysis of peration of bistable, monostable, and astable multivibrator cir- . The transition time and voltage waveforms which occur when gger pulse is applied to a conventional bistable multivibrator (or Eccles-Jordan trigger circuit) are analyzed in considerable detail. A similar analysis is carried out for the monostable circuit and for the multivibrator oscillator.

The final section of the book discusses certain basic types of blocking-oscillator circuits. The pulse transformer equivalent circuit is highly idealized by neglecting all capacitances. The operation of a triggered blocking oscillator using this very simplified equivalent circuit is analyzed, and the free-running case is then surveyed briefly.

The book is evidently intended for practicing engineers who have little or no familiarity with the methods of analysis of vacuum tube switching circuits. The use of Heaviside's operational calculus and the great detail with which some problems are treated detract somewhat from the desirability of the book as a reference for students.

William H. Surber
Princeton University
Princeton, N. J.

Basics of Digital Computers—John S. Murphy. (John F. Rider Publisher, Inc., New York, N. Y., 1958. 372 pp.)

This is definitely not just another book about computers. It is unique primarily because of the excellence of the style of presentation and also because of the completeness of the over-all selection of topics. The author has been very successful in writing a book which is excellent for its proposed use in training "computer technicians and field engineers." Professionals in the computer field will undoubtedly find the book insufficient for their needs since it is essentially descriptive in character and does not present specific or mathematical discussions. Also, the pictorial nature of the presentation ("at least one big illustration is given on each page") is likely to make an unfavorable initial impression on a professional. In spite of these facts, anyone interested in digital computers will probably find something valuable and interesting in this book. These considerations, coupled with the low cost ($7.50 paperbound, $8.50 clothbound), make this book a recommended addition to anyone's collection of computer literature.

The internal workings of a digital computer form the subject matter of this book with only a very minimal description of programming considerations. It is unfortunate that no mention is made of analog computers to fill out the introductory material. Also the author's handling of the difference between electron flow and current flow tends to be confusing at times—especially since the book is mainly intended for readers who are not engineers. On page 1-19 the rather misleading statement that "Like the relay, the flip-flop was found suitable for control functions, but not for storing data, *for it had only two states*" is made. There is an error in the figure on page 2-30; in the upper right hand corner of this figure the +20 v should actually be −20 v.

E. J. McCluskey, Jr.
Princeton University
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PILOT—A New Multiple Computer System—A. L. Leiner, W. A. Notz, J. L. Smith, and A. Weinberger. (*J. Assoc. Computing Mach.*, vol. 6, pp. 313–335; July, 1959.)

PILOT, now under construction at the National Bureau of Standards, is a one-megacycle, vacuum-tube computer system using modified SEAC circuits and small, one-microsecond, diode-capacitor memories. The system comprises three independently programmed computers. The first is a general-purpose scientific and business computer whose performance appears to be somewhat higher than that of a Transac S-2000 (with 12 μsec memory) and about half that of the Univac Larc. The second is specialized for very high speed index manipulation and similar housekeeping operations. The third computer, or Format Controller, uses a plugboard-stored program to effect input-output buffering and assembly together with simple character-by-character editing functions.

The authors briefly but adequately describe the formats, operation lists, and operation times for each of the three rather different computers whose internal organizations are not discussed. The extensive discussion of the novel over-all system organization and of the carefully-designed communications among the computers and with the environment is informative but sometimes prolix and occasionally vague (*e.g.*, the size of the primary computer's memory is not stated).

The described justification for PILOT is two-fold:

1) NBS needs an unusually flexible and rather powerful tool for investigating large-scale business data processing and simulating data processing devices.
2) The NBS group, believing that important real-time problems can best be attacked by networks of computers, desires to experiment with these.

The design itself indicates a preoccupation with the latter objective. It is highly questionable, for example, whether the use of an independent secondary computer is the easiest or most efficient way of performing housekeeping in parallel with computation; but this approach will undoubtedly yield more knowledge of computer networks. Similarly, the needs for versatility and efficiency in simulation are only superficially met in the principal computer. For example, binary floating point operation is augmented by decimal floating point operation, a feature whose low cost nevertheless exceeds its value. But, more fundamentally, the three-address instruction is ill-adapted for simulating other machines; and, most crucially, only rudimentary provisions are made for manipulating arbitrary groups of bits.

The tertiary computer, however, represents a sound generalization of current techniques of input-output control. Its programmability should indeed permit the easy attachment of a wide variety of input-output devices.

In short, this informative paper describes a machine which is likely to stimulate good work in the design and operation of computer networks but which does not seem peculiarly apt for investigating governmental data processing problems.

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Programming for Digital Computers—Joachim Jeenel. (McGraw-Hill Book Co., Inc., 1959.)

At last someone has had the courage to put out a book which deals honestly with the difficulties of programming for digital computers. Here is a systematic presentation of the standard detailed problems one encounters when programming a computer directly in machine language. Jeenel has taken great pains to give as lucid an exposition as may be possible for an admittedly difficult subject, and his efforts have been materially enhanced by the fine typographic work which has been accorded his flow diagrams. Both he and the publishers are to be congratulated. The author has avoided the mistake of getting involved with the intricacies of a particular computing machine, and his exposition is couched in terms of a rather well-behaved single-address hypothetical machine. Only in the first three chapters where he is considering the nonessential details of "how a computer really works" is there any real involvement with much that looks like machine language. The bulk of the book is therefore free to concentrate on the ideas involved in table lookup, sequencing, sorting, automatic address modification, etc.

This reviewer has a minor quibble with the author over his grouping of assembly and compiling systems. Such a treatment leaves the quite erroneous impression that these two categories are comparable in their sophistication and in their ease of execution or even construction. Also, the author only discusses pseudo-codes and external languages briefly toward the end of the book—along with other important topics such as testing and debugging programs. One might hope that in a book of 500 pages it would be possible to treat the question of external languages more thoroughly. Their importance has increased and is still increasing as people realize the cost of mistakes in writing programs in a language psychologically unsuited to the person doing the coding. On the other hand, this reviewer has just finished giving some lectures on programming and coding and he is all too well aware of the necessity for redundant exposition. In the light of that experience he cannot honestly wish that this book had been more tersely written. It is a fine book for those who wish to roll up their sleeves and learn how to code. Those who merely wish to add a computer veneer to their technical vocabulary would be well advised to stay away.

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Algebraic Topological Methods for the Synthesis of Switching Systems, Part III, Minimization of Nonsingular Boolean Trees—J. Paul Roth and E. G. Wagner. (*IBM J. Res. & Dev.*, vol. 4, pp. 326–344; October, 1959.)

This paper is concerned with the minimization of single output circuits which are disjunctions of trees of any desired set of logical elements. In any particular tree no input is allowed to appear more than once. Expressed alternatively, the authors consider "OR-ing" together of single output circuits, each of which is composed of arbitrary logical elements. These elements may have any number of inputs but only one output, which may drive one subsequent element. The circuits are restricted to be nonsingular. That is, no basic input variable may appear more than once in any one of these circuits.

The arbitrary elements are permitted to have various costs, and an algorithm is given for producing a minimum-cost circuit of the above type which realizes any given logical function. It is shown that this algorithm is much more efficient than some systematic exhaustive procedure. Nevertheless, there are still several lengthy, laborious phases of the algorithm which limit its usefulness. It would be interesting to determine whether the algorithm satisfies the authors' requirement that "the algorithm, when programmed on the IBM 704, should be capable of solving, say, an 8-variable problem with eight hours of machine time."

The basic steps given for producing a minimal circuit are:

1) Determination of the set of all nonsingular circuits whose disjunction is the given logical function.
2) Elimination of certain nonsingular circuits which cannot be members of any final minimum-cost circuit by means of an operation using what the authors call the "less-than relationship." This step may be combined with the first step.
3) Selection of certain nonsingular circuits (extreme nonsingular circuits) which must appear in any final minimum-cost circuit.
4) Determination by means of a process called branching of the remaining nonsingular circuits whose disjunction with the extreme nonsingular circuits constitutes a minimal-cost circuit.

Step one appears to be the most time-consuming and exhaustive, working from a matrix equivalent to the truth table of the given logical function. When combined with step two, it gives a set of functions analogous to Quine's prime implicants but more general, including them as a special case. Steps three and four are nearly identical to corresponding procedures from normal form minimization. It should be noted that several procedures exist in the literature[1–3] as alternatives to the branching operation.

One misprint was noted. On page 337 matrix K should be one not zero, in the second column and either in the first or third row. A novel feature of this paper is the parallel treatment of the material by the two authors in two complementary versions, a mathematical version and an engineering version. This was done with considerable success and might well be considered by other authors in areas of joint interest to engineers and mathematicians.

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AF Cambridge Res. Center
Bedford, Mass.

[1] M. J. Ghazala, "Irredundant disjunctive and conjunctive forms of a Boolean function," *IBM J. Res. & Dev.*, vol. 1, pp. 171–176; 1957.
[2] T. H. Mott, "Determination of the Irredundant Normal Forms of a Truth Function by Iterated Concensus of the Prime Implicants," Symp. on Switching Algebra, Internatl. Conf. on Information Processing; June, 1959.
[3] S. R. Petrick, "A direct determination of the irredundant forms of a Boolean function from the set of prime implicants," AFCRC, Bedford, Mass., TR-56-110, April, 1956.

On the Classification of Boolean Functions—Solomon W. Golomb (IRE Trans. on Circuit Theory, vol. CT-6, Special Suppl., pp. 176–186; May, 1959.)

Logic Matrices and The Truth Function Problem—Douglas F. Netherwood. (*J. Computing Mach.*, vol. 6, pp. 405–414; July, 1959.)

Both of these articles deal with the classification of Boolean functions and the derivation of standard forms for them. Two Boolean functions of n arguments are said to be *equivalent* whenever one can be transformed into the other by operations of 1) permuting arguments, 2) complementing arguments, 3) complementing the function

re are $2^{n+1} \cdot n!$ distinct transformations to be considered, and these ition the set of functions of n arguments into disjoint *equivalence es* of mutually transformable functions. If f and g are equivalent tions, the derivation of a circuit for g from a circuit for f is trivial, early so, once the appropriate transformation is known. Equiva- relationships are conveniently investigated by defining for each valence class a representative member, or *standard transform*, and ng an algorithm for reducing an arbitrary function to the stand- transform of its class. Two functions are then equivalent if and if they reduce to the same standard transform.

Let a *k vector* be defined as an ordered k-tuple of elements, each 0 , and let the *distance* between two k vectors be the number of es in which corresponding components have different values. One esentation of a Boolean function f of n arguments is given by the of n vectors corresponding to configurations of argument values which f has value 1. The distance relationships among the n vec- of this set are essentially invariant under transformations of the considered; hence, they provide a means for function classifica- . Netherwood shows how these relationships can be used to define dard transforms, by imposing certain requirements on the order which they appear when the n vectors are listed in a prescribed ner. The reduction of a given function to its standard transform, ever, may involve rewriting the matrix of n vectors several times; , there are cases where it is difficult to recognize when the stand- transform has, in fact, been obtained. Since only vectors corre- ding to function values 1 enter the procedure, the method should articularly applicable whenever the total number of 1 values for function (or its complement) is relatively small.

Another general way of representing a Boolean function f of n uments is as a 2^n vector, whose components give the function val- associated with the 2^n configurations of argument values, listed a prescribed order. The classification criteria introduced by omb involve the distance relationships between the vector f and vectors of a particular set of 2^n functions. This set is obtained by ng all possible modulo 2 sums of 0, 1, $\cdots$, n arguments. It forms sis for generating the set of all 2^n vectors, when the latter is con- ed as a linear space with operations of modulo 2 addition and tiplication.

The 2^n distances between the vector f and the 2^n basis vectors are to define invariants for transformations of permutation and plementation. The fact that the basis vectors correspond to a plete set of orthogonal expansion functions shows that the set of riants uniquely characterizes f. A standard transform is then ned by imposing ordering requirements on the list of invariants. standard transform is obtained in stages, and at any stage several sforms of the function may have to be considered. Since it is al- s necessary to work with 2^n vectors, and a set of 2^n invariants, the x involved in implementing the procedure increases rapidly as n eases. Golomb indicates how aids in the form of charts and tem- es can be employed to simplify the task.

Both the Netherwood and Golomb procedures make use of funda- tal properties of Boolean functions; the articles therefore are vant to the general investigation of Boolean function structure. use by Golomb of the theory of expansion in terms of an orthog- system is particulary noteworthy.

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lysis of Bilateral Iterative Networks—F. C. Hennie. (IRE Trans. Circuit Theory, vol. CT-6, pp. 35–45; March, 1959.)

This paper is the first general treatment of bilateral iterative com- tional networks to appear in print. Methods involving a number ovel concepts are given for analyzing, simplifying and synthesiz- such networks. The paper is clearly written, and well worth read- for those interested in either the design or theory of switching orks.

An iterative combinational network consists of a chain of identical . Each cell is a combinational network. Each cell in a bilateral iterative network has an input from a cell on its left and from a cell on its right. It also has a primary input. These inputs taken together constitute the "total state" of the cell, and determine the cell's outputs, which are the left, right, and primary outputs. A cell table of combinations giving for each possible "total state" all the cell outputs, together with boundary conditions (inputs to end cells) constitute the starting point of the analysis. The end of the analysis is a reasonably simple system for determining for any set of primary inputs to a network built of such cells, what the set of primary outputs will be.

The author notes that if cell A is in total state S_1,B, the adjacent cell on A's right can be in state S_2 if the right output of S_1 is the left input of S_2, and (since the network is assumed to be in equilibrium) the left output of S_2 equals the right input to S_1.

Starting then with the set of total states possible in the leftmost cell (determined by the left boundary conditions) and labelling this set a_0, one may determine the set of total states possible to the cell on its right, for each primary input of the leftmost cell. This new set is given a new label if it is different from a_0. By continuing the above process one may construct a *left label matrix*, which contains for each possible label, the label which will result, for each possible primary input. Starting with the right boundary conditions a right label matrix can be similarly constructed.

With simple tests on these matrices the author shows how to determine if the network does, in fact, have an equilibrium condition for every set of primary inputs, and whether the network's output is independent of its history. The left and right label matrices together with an output matrix which gives the primary output of a cell for every pair of labels, one left, and one right, allows one to determine simply the primary outputs of the network for any set of primary inputs. It is further shown that the left and right label matrices each define a unilateral iterative network. These two unilateral networks together with an output network described by the output matrix make up a network which is equivalent to the original bilateral network. If the two unilateral networks are minimized by removing redundant states in each of them, we have a canonical description and an associated canonical network for the bilateral network. Canonical here means that any two bilateral networks having identical canonical descriptions are equivalent. This is what the author calls his fundamental theorem.

Although the removal of redundant states of a cell in a unilateral iterative network can be carried out with the same processes as those used in synchronous sequential circuits, a new process is required in the case of cells of bilateral iterative networks. The author describes this process, which follows, in a way, analogously to that for sequential circuits, from his definition of coredundancy. Roughly two states are coredundant if the replacement of the outputs of one for the outputs of the other in the cell table of combinations leads to a network equivalent to the original bilateral network.

Finding the minimum state description of the cell of a bilateral network turns out to be more difficult than for the cell of a unilateral network. This results largely from the fact that coredundancy is not an equivalent relation, and therefore the number of states which can be removed is a function of the order in which states are removed.

The author points out a number of areas which require further study. For instance his analysis assumes equilibrium in the bilateral network. How it gets there, or its transient behavior, is still a problem. As the author points out, however, there are a number of network forms which, although not necessarily minimum in any sense, will guarantee realization without any transient problems. The canonical network is one of these. Another open problem not mentioned by the author concerns the special conditions which may be exhibited by cells near the ends of the bilateral network. For instance, there may be states which are accessible to cells near the middle of the network which are not accessible to those at the ends.

The author gives a proof of his fundamental theorem, and an outline of a proof of the process for detecting coredundancy. On the other hand a number of equally important points get only sketchy treatment. Perhaps the paper should have been longer.

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Abstracts of Current Computer Literature

(THROUGH OCTOBER, 1959)

These abstracts and the associated subject and author indexes were prepared on a commercial basis under the direction of Dr. Geoffrey Knight, Jr., who also publishes the abstract journal "Semiconductor Electronics." Local volunteer support of this endeavor has been furnished by Messrs. P. R. Bagley and R. P. Mayer of The Mitre Corporation, and F. E. Heart of Lincoln Laboratory, M.I.T.

Additional copies of these abstracts are available from IRE Headquarters, 1 East 79th St., New York 21, N. Y., at $1.00 per copy, or $3.50 for the set of four to be published in 1960.

—*The Editor.*

-1: EQUIPMENT—THEORETICAL DESIGN

ching Circuits Using Bi-Directional linear Impedances, by T. B. Tomlinson nputer Developments Ltd.); *J. Brit. E*, vol. 19, pp. 571–591; September, 1959.

n a brief general review of logic cir-y, a case for a bi-directional, nonlinear ching element is developed. In order to pare circuits using such elements with e using standard semiconductor diodes, main features of diode gates are con-red in detail. Particular attention is paid ie design of *p-n-p* transistor driver stages their dependence on the logic sequence. uits using bi-directional "constant volt- elements, including a "two-decision" D gate, are described. Possible types of tant voltage element are discussed and rimental results for multi-electrode sili-carbide devices are given. An interesting ure of the latter is the nonlinear be-or of capacitance. An attempt is made ompare gating circuits employing con-t voltage, bi-directional elements with dard diode gates from performance/cost, t of view. A majority is made possible "constant current," bi-directional ele-t. If one input is used as a control, gate can be controlled to act as a 3-AND, R, or a "2 or more out of 3" logical unit out change of input or output connec-s. Some possible realizations of the con-t current device are discussed. A binary-decoder circuit and a simple binary-full r circuit are given as examples of the ication of the nonlinear elements and to trate their unusual features.

rowave Computer Research, by M. P. er (G.E. Microwave Lab.); *U. S. Gov. Rept.*, vol. 32, p. 359(A), September 11, 9; PB 136 999 (order from LC mi $3.30, 7.80).[1]

A detailed analysis of mμsec pulse trans-ion is carried out by means of the rier transformation. Gaussian pulse en-pes are assumed as a reasonable approxi-ion to physically realizable pulses. Pulse rioration due to amplitude and phase ortion (dispersion) is calculated and ussed.

ogic Design for a Microwave Computer, S. P. Frankel (G.E. Co.); IRE TRANS. ELECTRONIC COMPUTERS, vol. EC-8, pp. -276; September, 1959.

The special problems which arise from use of microwave components such as elling-wave tubes and waveguides in a computer are discussed and the logic design for a microwave computer is developed with attention to these problems.

A-2: EQUIPMENT—COMPONENTS AND CIRCUITS

546

Design Criteria for Autosynchronous Circuits, by J. C. Sims, Jr. (Sylvania Elec. Products, Inc.) and H. J. Gray (Univ. of Pennsylvania); *Proc. Eastern Joint Computer Conf.*, pp. 94–99; December 3–5, 1958.

The speed limitations of synchronous computers are discussed and design criteria for higher speed operation are presented. Examples for a logic and circuit organization which results in both faster operation and improved performance to cost ratios are given. In particular, circuits which are free of transient logical malfunctions, sometimes called "spikes," are developed and a typical autosynchronous system is shown.

547

Microminiature Electronic Circuitry for Space Guidance, by E. Keonjian (Amer. Bosch Arma Corp.); 1959 IRE WESCON CONVENTION RECORD, pt. 6, pp. 92–99.

The results of a feasibility study of microcircuitry as applied to one part of a space guidance digital computer is described. A full adder consisting of seventeen individual circuits has been built within a total volume of 0.5 cubic inch as one phase of this study. This corresponds to a final circuit parts density of approximately 300,000 parts per cubic foot. Various layouts of components and interconnection techniques were utilized in the attempt to reach a workable compromise between standardization and optimization. In all circuits the active elements are directly integrated into the circuit substrate. Various concepts of microminiaturization are briefly described, the basic circuit requirements for space electronics are outlined, and the future objectives of the microminiaturization program are given.

548

Data Storage and Display with Polarized Phosphors, by H. P. Kellmann and J. Rennert (New York Univ.); *Electronics*, vol. 32, pp. 39–41; August, 1959.

The application of persistent internal polarization (p.i.p.) in organic and inorganic phosphors and in single crystals such as cadmium sulphide to photography and to the storage of data in computer memories is discussed. Data is stored by separating charges in the material with dc fields and radiation. Two techniques for reading out the data are described. The preparation of the p.i.p. layers and the mechanisms involved in their operation are discussed.

549

An Approach to Microminiature Printed Systems, by D. A. Buck (M.I.T.) and K. R. Shoulders (Stanford Res. Inst.); *Proc. Eastern Joint Computer Conf.*, pp. 55–59; December 3–5, 1958.

A technique for producing microminiature printed circuit conductors which are 0.1 micron wide is described. Such a technique permits the fabrication of microminiature circuits with a component density of 50 million per square inch per layer. A thin metallic film is formed on a substrate by vacuum evaporation or by vapor plating, a resist is produced on desired areas by the free radical polymerization of siloxane or hydrocarbon vapors, the exposed metallic film is removed by vapor etching, and the resist is then removed by hydrogen fluoride vapor. The resist may also be heated to form an insulator between metallic layers. The technique is illustrated by the etching of a molybdenum film (on a silicon monoxide film) about 800 Angstroms thick into squares about 0.001 inch on a side. Techniques for producing desired patterns in the resist are discussed.

550

Research on Automatic Computation Techniques and Components, by W. M. Becker, R. W. Clark, and M. S. Hall (Natl. Cash Register Co.); *U. S. Gov. Res. Repts.*, vol. 32, pp. 359–360(A), September 11, 1959; PB 151 834 (order from OTS $3.00).[1]

The implementation of a notation scheme designed to serve as the arithmetic unit of a digital computer is discussed. The principal problems were those of finding a method of operating magnetic core function matrices faster and more reliably than was possible heretofore, and to devise a way of operating large (10^6 bits) magnetic core matrices at high speeds without the necessity of redundant circuitry. A study of methods of processing vacuum evaporated barium titanate films which might lead to ferroelectric behavior suitable for computer device application is also presented. Problems encountered in the formation of thin films of ferroelectric material other than barium titanate are discussed. Finally, the fabrication of a fast electro-optical switch for logic circuitry in digital data processing systems by using the optimum combination of polycrystalline electroluminescent (EL) and photoconductive (PC) materials is described. ZnS-type EL phosphors and CdS, CdSe, and PbS PC materials were investigated. The following problems are considered: 1) the effects of the dielectric characteristics of the embedment on the properties of an EL layer; 2) the spectral emission of the EL materials and the spectral sensitivity of the PC materials; and 3) the speed of response of the EL layer and the PC element.

551

Using Inductive Control in Computer Circuits, by W. M. Carey (Minneapolis-Honeywell Regulator Co.); *Electronics*, vol. 32, pp. 31–33; September 18, 1959.

Transistorized digital computer time-measuring circuits which utilize inductance as the passive time-measuring or storage element are discussed. The circuits include a differentiator, a single-shot multivibrator which provides output pulses longer in duration than the input trigger, a self-starting choke-controlled free-running multivibrator, a transformer-controlled free-running multivibrator, a counter circuit which uses conventional linear transformers instead of the usual square hysteresis loop core, and a shift register. The advantages of inductance over capacitance control are pointed out. All these circuits have been utilized in a commercial data processor for several thousand hours without a component or computational failure of any kind.

[1] U. S. Government Research Reports may be or-d by prepayment of the fee to the organization ated. When ordering, give the complete title PB number of the report. Mi indicates microfilm, dicates photocopy.
LC indicated, write to: Library of Congress, oduplication Service, Publications Board Project, hington 25, D. C. Make check or money order ble to: Chief, Photoduplication Service, Library ngress.
OTS is indicated, write to: Office of Technical ces, U. S. Department of Commerce, Washing-25, D. C., or to any Department of Commerce office. Make check or money order payable to: , Department of Commerce.

552
Transistor Blocking Oscillator for Use in Digital Systets, by A. A. Kaposi (Ericsson Telephones Ltd.); *Electronic Engrg.*, vol. 31, pp. 480–484; August, 1959.

A transistor blocking oscillator circuit which utilizes a saturable transformer to produce a pulse length that is independent of transistor parameters, of temperature, and of load current is described. Practical circuits having pulse lengths of 1.5 μsec and greater have been constructed. The circuit is particularly suitable for driving magnetic core counters.

553
Analysis of TRL Circuit Propagation Delay, by W. J. Dunnet, E. P. Auger, and A. C. Scott (Sylvania Elec. Products, Inc.); *Proc. Eastern Joint Computer Conf.*, pp. 99–108; December 3–5, 1958.

Experimental and analytical investigations of the propagation delay in a transistor-resistor logic (TRL) circuit are discussed. Propagation delay is the time required, after the application or removal of an input signal, for the TRL transistor output level to begin to change. Transistor input capacity; transistor rise, decay, and storage times; and their relationship to propagation delay are discussed. A procedure for calculating the propagation delay for a given transistor and circuit configuration is outlined. TRL circuit environment is considered and general expressions relating turn-on and turn-off circuit beats to circuit parameters (supply voltages, input and collector resistors) and transistor steady-state voltages, V_{BE} and V_{CE} (saturated) are developed. A computer program based on these relationships is being prepared in order to achieve optimum TRL circuit design and to compile propagation delay tables useful to the logical designer.

554
DC Design of Resistance Coupled Transistor Logic Circuits, by W. J. Wray, Jr. (Burroughs Corp.); IRE TRANS. ON CIRCUIT THEORY, vol. CT-6, pp. 304–310; September, 1959.

Worst-case dc design equations for resistance coupled transistor logic circuits are presented and discussed. A solution is chosen in a form which provides for setting switching transient times in advance of calculating the dc design. All constants are discussed, and the algebraic solution is obtained for values of the unknown resistors and voltages. A numerical example illustrates a typical design with five inputs and five outputs, using the type GT-759 transistor.

555
Millimicrosecond Digital Computer Logic, by N. F. Moody and R. G. Harrison (Defence Res. Board of Canada); *Electronic Engrg.*, vol. 31, pp. 526–529; September, 1959.

A transistorized fast-pulse logic system which utilizes transformer coupled stages and is tolerant to digit delays is described. The transistors may be saturated without significant loss in speed. Logical circuits for OR, AND, INVERTOR, and RE-CLOCK are presented, together with a driver which permits a "fan out" factor of 5. Existing logical units an chandle 1.2×10^7 digits per second. This figure can be improved to 2×10^7 digits per second. Since the speed of a logical unit is one half the potential data handling speed of the system, a speed of 4.0×10^7 digits per second is possible.

556
Direct-Coupled Transistor Logic Circuitry, by J. R. Harris (Bell Tel. Labs, Inc.); IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-7, pp. 2–6; March, 1958.

Logical design rules and transistor specifications for direct-coupled transistor logic circuitry are enunciated. Typical circuit configurations, reliability, temperature limitations and speed of operation are discussed. Silicon transistors are considered to be less susceptible to false switching due to noise than germanium transistors. The properties of DCTL circuitry lend themselves readily to the design of complete systems.

557
Nanosecond Logic by Amplitude Modulation at *X* Band, by W. C. G. Ortel (Bell Tel. Labs. Inc.); IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-8, pp. 265–271; September, 1959.

A basic circuit which consists of a diode modulator controlled by the signal from a diode detector and which can perform logical AND, EXCLUSIVE-OR, and OR functions upon pulsed microwave signals is described. Pulse rates up to 500 mc have been used at a carrier frequency of 11,000 mc. To cemonstrate that microwave circuits can be used for the regeneration and circulating storage of pulses, as well as for logic, a digital arithmetic unit has been built which multiplies two 8-digit binary numbers. Various forms of the basic circuit have been studied in operation.

558
Microwave Logic Circuits Using Diodes, by W. Sauter and P. J. Isaacs (Sperry Gyroscope Co.); IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-8, pp. 302–307; September, 1959.

A method of controlling the transmission of microwave power in a waveguide via external control of the dc bias on a semiconductor diode mounted across the waveguide in a direction parallel to the *E* field is discussed. The combination of a microwave detector with such a modulator affords a means whereby RF power in one waveguide can be made to control RF power in a second waveguide. In order to test the applicability of this circuit to binary logic functions, a regenerative memory loop has been constructed. Travelling-wave tubes were employed to raise the level of a controlled signal to that required by the detector. Using an *X*-band carrier, binary pulse stability was observed at pulse repetition rates of 685 mc.

559
Fast Microwave Logic Circuits, by D. J. Blattner and F. Sterzer (RCA); IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-8, pp. 297–301; September, 1959.

The representation of binary information in a carrier-type digital computer system by the presence or absence of an RF pulse in a given time interval is discussed. Using strip-line printed circuit technique and point-contact diodes, passive AND an NOT gates which operate with RF pulses o less than 2 mμsec duration (*i.e.*, an effectiv pulse repetition rate of 500 mc) at a carrie frequency of 3000 mc have been constructed The basic gates were combined to form hal adders. Unlike other carrier approaches these circuits keep the information in R form through all steps of the logic opera tions; *i.e.*, both inputs and outputs of a elements are RF pulses.

560
The Parametron, A Digital Computing Element Which Utilizes Parametric Oscillation, by E. Goto (Univ. of Tokyo); PROC IRE, vol. 47, pp. 1304–1316, August 1959 p. 1840, November, 1959.

The basic principles and applications o the parametron digital computer element ar described. A parametron element is esser tially a resonant circuit with a nonlinea reactive element which oscillates at one-ha the driving frequency. The oscillation used to represent a binary digit by th choice between two stationary phases radians apart. The basic principle of logica circuits using the parametron is explained and research on and applications of param etrons in Japan are described.

561
Microwave Parametric Subharmonic Oscillators for Digital Computing, by F. Sterze (RCA); PROC. IRE, vol. 47, pp. 1317–132 August, 1959.

In a digital information handling syste a binary one can be represented by an R signal of a given phase, frequency, and am plitude, and a binary zero by a signal of th same frequency and amplitude but wit opposite phase. The use of subharmonic o cillators to switch, store, and amplify binar information coded in this manner is re viewed. A variable capacitance subharmon oscillator having an output frequency 2000 mc is described, and the use of this o cillator in circuits for amplifying, scalin and performing logic functions is discussed The circuits described operate at pulse rep tition rates exceeding 100 mc. By raising th carrier frequency to *X* band, it should be po sible to increase the maximum rate to a fe hundred megacycles.

562
Semiconductor Diodes in Parametric Subharmonic Oscillators, by J. Hilibrand an W. R. Beam (RCA); *RCA Rev.*, vol. 2 pp. 229–253; June, 1959.

The nonlinear reactance elements mo suitable for high-frequency parametric sub harmonic oscillators are semiconductor d odes. The performance of these diodes in th basic oscillator circuit is evaluated. The e fects of stray capacitance, spreading resis ance, junction conductance, and capac tance-voltage sensitivity are taken into a count in the analysis of theoretical oscillato performance. The subharmonic output vol age is limited, in oscillators designed fo minimum rise time, to values much less tha the pump voltage, but greater output vol ages can be obtained if rise time is sacrifice In such high-voltage operation, the ampl tude is limited by available power from th

np source and conversion efficiency is de-mined by spreading-resistance losses. e also the following abstract.]

niconductor Parametric Diodes in Micro-ve Computers, by J. Hilibrand, C. F. cker, and R. D. Gold (RCA Labs.); IRE ANS. ON ELECTRONIC COMPUTERS, vol. -8, pp. 287–297; September, 1959.

The parametric subharmonic oscillator rates by energy transfer from the pump quency to the oscillator frequency ough a nonlinear energy storage element h as the nonlinear capacitance of a semi-ductor diode. Both the requirements on diode for satisfactory performance in this uit and the limitations on oscillator per-mance which arise from the nature of the niconductor diode are examined. The lysis shows that abrupt junction diodes st have a Q of at least four at the oscilla-n frequency if there is to be any usable rgy transfer, and that graded junction des must have a Q of six. The time con-nt governing the rise of the envelope of subharmonic waveform is a marked ction of the stray capacitances; this func-n is examined in detail. The choice of bias tage to obtain the fastest possible rise e involves consideration of the stray acitance, the Q of the available diode, l limitations imposed by excessive pump ver requirements. For negligible stray acitance, it is shown that the subhar-nic waveform can rise by a factor e in 1.3 les of the subharmonic frequency for an upt junction diode, or in 1.9 cycles for a ded junction diode. The principles in-ved in the design of the semiconductor de are examined and the choice of ma-ials, impurity distributions, and fabrica-n techniques are discussed. A new diode apsulation intended for direct mounting microstrip transmission lines is described. equivalent circuit characterization, in ich the parameters may be directly re-ed to the diode structure, and several hniques for the measurement of these rameters are discussed.

rametric Phase-Locked Oscillator—Char-eristics and Applications to Digital Sys-ns, by L. S. Onyshkevych, W. F. Koson-cy, and A. W. Lo (RCA Labs.); IRE ANS. ON ELECTRONIC COMPUTERS, vol. -8, pp. 277–286; September, 1959.

The behavior and possible computer ap-cations of the variable-capacitance para-tric phase-locked oscillator (PLO), which erates readily at kilomegacycle frequen-s, are discussed. The steady-state behav-of the device is described; variation of output voltage with pump voltage, ding, tuning and frequency variations presented in the form of characteristic rves. Results indicate that the device is her insensitive to reasonable changes in erating conditions and parameter values. e transient behavior of the PLO shows at the device can be switched in a number different ways. Five such modes of opera-n are discussed: phase initiation, forced itching, burst generation, tri-stable opera-n, and unconditional switching. Each of ese modes has particular advantages for various applications. Switching times of the order of 3 to 10 cycles of the signal frequency are readily obtainable. The various modes of operation of the device suggest a number of applications both in logic and in memory. To illustrate the versatility of the device, a random access memory is described as an example.

565

BIAX High Speed Magnetic Computer Element, by C. L. Wanlass and S. D. Wanlass (Ford Motor Co.); 1959 IRE WESCON CONVENTION RECORD, pt. 4, pp. 40–54.

BIAX digital computer memory and logic elements are described. These elements are multi-aperture ferrite devices which utilize flux interference rather than the more conventional technique of flux steering. The hysteresis characteristics of the material are not critical and the devices operate over a wide range of temperature and at a higher speed than other magnetic devices. The BIAX memory element permits nondestructive readout.

566

Megacycle Magnetic ROD Logic, by D. A. Meier, B. A. Kaufman, and D. W. Rork (Natl. Cash Register Co.); 1959 IRE WESCON CONVENTION RECORD, pt. 4, pp. 27–31.

The application of the magnetic ROD in performing the logical switching functions necessary in a digital system is described. In the inhibit mode, the ROD is shown to be the electrical equivalent of the toroidal type magnetic core. The use of a sine wave clock is a particular feature of this technique which simplifies the distribution and phasing problems in a large system. Two-megacycle logical switching is described with a discussion of design and system applications.

567

Theory of a Fast-Switching Electron-Beam Frequency Divider, by N. M. Kroll and I. Palocz (IBM Watson Lab. at Columbia Univ.); *IBM J. Res. & Dev.*, vol. 3, pp. 345–354; October, 1959.

A velocity-modulated electron-beam microwave tube which can be operated as a frequency divider is described. Its operation is analyzed in terms of velocity-modulation bunching theory, neglecting space-charge forces. Because of the existence of two stable states opposite in phase, such a divider can be advantageously employed in a microwave logical system. The transient behavior of the device is discussed, particularly with reference to the time required to switch the device from one of its stable states to the other. Factors involved in the minimization of this time interval are analyzed.

568

Evaporated Films and Digital Computers, by D. W. Moore (Servomechanisms, Inc.); 1959 IRE WESCON CONVENTION RECORD, pt. 4, pp. 32–39.

The use of evaporated conductive, dielectric, and magnetic films in the construction of digital computer circuitry is discussed. The equipment necessary to carry out the evaporation processes is briefly described, the electron bombardment evaporation technique being stressed. Thin films result in a saving of space and in increased reliability. The various approaches to microcircuitry are described and an example of the use of the magnetic domain interaction phenomena in memory and logic equipment is presented.

569

A Glow Counting Tube Read-Out Technique and its Application, by S. K. Chao (Sylvania Elec. Products, Inc.); IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-8, pp. 317–320; September, 1959.

A technique whereby the content of a cold cathode counting or decade glow transfer tube is recognized and read out through a carrier signal applied to the anode and 10 detectors connected to the 10 cathodes is described. The readout is of the nondestructive type since it does not alter the content of the tube. A large number of glow tubes can be conveniently read out in this manner simply by connecting all corresponding cathodes together. The carrier signal is then successively distributed to their anodes. An example of such an application in which 19 channels of four glow tubes each are read into an IBM card punch is given.

A-3: EQUIPMENT—SUBSYSTEMS

570

The Research and Development of the Magnacard System, by A. M. Nelson (Magnavox Co.); *U. S. Gov. Res. Repts.*, vol. 32, p. 359(A), September 11, 1959; PB 151 828 (order from OTS $3.00).[1]

Methods for the high-speed handling of magnetic cards including all the necessary functions to permit automatic sorting, merging, selecting, filing, reading, and writing are discussed. A special magnetic card was developed to provide a reliable unit document record. The techniques developed utilized pneumatic means extensively, including vacuum drums to transport magnetic cards at 300 inches per second and high-speed electrodynamic air tubes for the selective transfer operations that formed the basis of card sorting and selection functions. Card feed control was also accomplished pneumatically, and reversible stations capable of either feeding or stacking cards were devised. Reading and writing of information to provide storage of up to 1000 decimal characters on cards 1 inch × 3 inches was accomplished.

571

Transistor Circuit Technique for a Core Memory with 500 Millimicrosecond Cycle Time, by V. J. Sferrino (M.I.T. Lincoln Lab.); 1959 IRE WESCON CONVENTION RECORD, pt. 4, pp. 3–15.

The "impulse switching mode" of driving ferrite memory cores is discussed. The method utilizes current pulses having large peak amplitudes and very short duration to overdrive the core and to "partially switch" the core, respectively. The technique reduces the switching and read-write cycle times of the ferrite memory cores by an order of magnitude or more over those obtained for the normal mode of drive. A transistorized memory which utilizes impulse switching techniques consists of 1040 words of 80-bit length is described. It is organized

as a linear selection, sequential access memory with a read-write cycle time of 500 millimicroseconds and a sequential word address time of less than 1 microsecond. The system provides access to almost 100 million bits per second. A drive circuit which utilizes two four-layer *p-n-p-n* diodes to generate the high current, short duration pulses necessary to drive the cores is described. The design of the sensing, logic, and additional drive circuitry for the system is also discussed.

572
Coincident-Current Magnetic Memory Unit, by W. N. Papain (M.I.T.); *U. S. Gov. Res. Repts.*, vol. 32, p. 229(A), August 14, 1959; PB 140 843 (order from LC mi $4.80, ph $13.80).[1]

Operation of a small, toroidal, ferromagnetic core whose B-H characteristic is properly "rectangular" in shape so that its flux polarity reverses only when the right combination of two or three magnetizing coils are coincidentally excited is discussed. The core may be used as a coincident-current binary memory device which might be assembled, with many others, into a two- or three-dimensional memory system. Selection within such a system would be accomplished by means of physical-line switching along the two or three space coordinates.

573
High-Speed, High-Capacity Photographic Memory, by C. A. Lovell (Bell Tel. Labs. Inc.); *Proc. Eastern Joint Computer Conf.*, pp. 34–38; December 3–5, 1958.

A high-speed, high-capacity flying spot photographic permanent memory of 10 million bit capacity and 5-μsec random access time is described. Reading and writing is achieved by servopositioning a light beam obtained from a cathode ray tube. One plate of a $(256)^2$-word memory covers a $6\frac{1}{4}\times 6\frac{1}{4}$ inch area. Possible applications are in machine language translation, solution of logical problems, table look-ups, and storage of subroutine libraries.

574
ORACLE Curve Plotter, by C. T. Fike (Oak Ridge Natl. Lab.); *Commun. Assoc. for Computing Mach.*, vol. 2, pp. 38–39; October, 1959.

ORACLE, a cathode ray tube curve and character plotter, is briefly described. Resolution is sufficiently fine to permit the use of both upper and lower case characters. The 1024×1024 grid is divided into an array of smaller rectangles, each point in which is correlated with a bit in a binary word. A 0 bit indicates that the corresponding point is not to be brightened, a 1 bit that it is.

575
Converter, Analog-to-Digital, Digital-to-Analog, CV-710/U, (Packard-Bell Computer Corp.); *U. S. Gov. Res. Repts.*, vol. 32, p. 360(A), September 11, 1959; PB 140 851 (order from LC mi $3.90, ph $10.80).[1]

A device which receives a voltage input and generates a proportional binary number as an output is described. There is an increment, a decrement, or no change in the digital number as the input varies. The changes are also available as output. A reverse mode of operation receives a serial binary number as an input and generates a proportional voltage as an output.

576
Bufferin' is Aspirin for EDP Headaches, by E. Jacobi (Litton Industries); *Computers and Automation*, vol. 8, pp. 30–32; September, 1959.

The operation of an all-transistorized core buffer capable of operating at frequencies up to 100 kc (10 μsec per character) is described. Various applications, such as magnetic tape to paper tape conversion, series-to-parallel conversion, and high-speed printing are outlined.

577
A Versatile Character Generator with Digital Input, by E. D. Jones (Stanford Res. Inst.); 1959 IRE WESCON CONVENTION RECORD, pt. 4, pp. 16–20.

A device which will generate alpha-numeric characters and symbols from six-wire parallel binary character-sequential input information is described. The character generation is accomplished in a monoscope tube containing an aluminum target on which all of the characters and symbols are printed in an 8×8 matrix. A small raster sufficient in size to cover one character is generated. The raster is deflected to the desired character by the decoded digital input signal. The video waveform present at the monoscope target, when used to intensity modulate a synchronously-swept CRT display device, writes the character on the face of the tube. This signal may also be employed to drive certain types of hard copy printers. Additional deflection potentials are used to position the character in the desired display format. Simple and reliable semiconductor circuitry for accomplishing the required indexing and scanning functions are described.

578
Character Display System for Use as Digital Computer Output, by P. V. S. Rao (Tata Inst. of Fundamental Res., Bombay, India); *Rev. Sci. Instr.*, vol. 30, pp. 749–750; August 1959.

A system in which the output of a digital computer is displayed as an arbitrary character on a memotron tube is described. Two sequences of pulses, each consisting of 16 pulses equally spaced in time, each either positive or negative, and all of equal magnitude, are applied to X and Y counters. Each pulse either increases or decreases the contents of the counters by one. The digital data in each counter is then converted to analog data which is applied to the deflection plates of the tube. Eight types of basic lines are traced on the screen and the characters are built out of these basic lines by continuously tracing them one after another in the proper sequence. The method for obtaining the pulse sequences is described. Typical characters are shown. Some advantages of the system are: a) it does not involve any critical and complicated adjustments, b) the shape of characters can be easily changed, c) the operation of the system is mainly digital, and d) the character is written as a continuous trace.

579
Burroughs Truth Function Evaluator, by W. Miehle (Univ. of Pennsylvania); *J. Assn. for Computing Mach.*, vol. 4, pp. 189–19 April, 1957.

A relay truth function evaluator capab of evaluating all the logical combinatio of up to 10 variables is described. The fur tion must be written in the parenthesis-fr notation of Lukasiewicz, as this notati has been found convenient to mechani It is possible to evaluate a tautology length 98 and rank 6 in 10 variables in hours. The device is particularly valuable f testing the equivalence of simplifications a formula to its original form.

580
An Error Correcting Encoder and Decod for Phone Line Data, by K. E. Perry (M.I. Lincoln Lab.); 1959 IRE WESCON Co VENTION RECORD, pt. 4, pp. 21–26.

Following a brief discussion of the Ree Muller error detecting and correcting cod the block diagrams for an encoder and a d coder which can be used with this code a described. The equipment can encode a 6 bit word into a 128-bit word and correct to seven errors per word. It is also possib to encode binary sequences thousands bits in length.

581
Electronic Probability Generator, by G. N White (G. E. Res. Lab.); *Rev. Sci. Inst* vol. 30, pp. 825–829; September, 1959.

An electronic probability generator, EP which can be used to study nonstationa random processes is described. The EPI c electronically "flip" a coin at a maximu rate of 500 times/second. The probability heads of this electronic coin can be vari from 0 to 1 and is a linear function of the i put voltage. Graphs which illustrate t ability of EPI to generate independe events are presented. EPI can also be us to generate sequences of heads and ta controlled by higher order probabilitie The only additional equipment required an electronic switch.

A-4: EQUIPMENT—DIGITAL COMPUTERS

582
Decimal-Binary Conversions in CORDI by D. H. Daggett (Convair); IRE TRAN ON ELECTRONIC COMPUTERS, vol. EC-8, p 335–339; September, 1959.

A special-purpose, binary comput called CORDIC (COordinate Rotation DI tal Computer) which contains a uniq arithmetic unit composed of three sh registers, three adder-subtractors, and su able interconnections for efficiently perfor ing calculations involving trigonomet functions is described. A technique for ing the CORDIC arithmetic unit to conv between angles expressed in degrees a minutes in the 8, 4, 2, 1 code and angles pressed in binary fractions of a half revo tion is formulated. Decimal-to-binary c version is accomplished through the gene tion of an intermediate binary code in wh the variable values are $+1$ and -1. Each these intermediate code variables contr the addition or subtraction of a particu binary constant in the formation of an

nulated sum which represents the angle. amples are presented to illustrate the hnique. Binary-to-decimal conversion is omplished by applying essentially the ne conversion steps in reverse order. Fun- nental principles of the conversion tech- ue, rather than details of implementa- n, are emphasized. The CORDIC conver- n technique is sufficiently general to be plied to decimal-binary conversion prob- s involving other mixed radix systems l other decimal codes. (See also Abstract .)

A-5: EQUIPMENT—ANALOG COMPUTERS

3

e Space Card: A Two-Dimensional Func- n Generator, by C. M. Jones and G. Har- l (A.F. Cambridge Res. Center); *U. S. . Res. Repts.*, vol. 32, p. 227(A), August 1959; PB 151 524 (order from OTS $0.75).[1]

The space card, a printed-circuit card ered with a thin even film of hard resis- e material, is discussed. A predetermined metric electric field results when the card lectrically excited at several points. When e magnitude of the electric field is made a nction of its physical position, the func- n is two-dimensional and can be read out positioning a brush contact on the card. e technique is especially applicable to o-dimensional analog function generation analog computation. The physical and ctrical characteristics of the space card, thods of construction, theory of excita- n, life-testing, and its advantages and advantages are described. Accuracies to per cent, long life, and stable operation ve been achieved.

4

e Design of Position and Velocity Servos Multiplying and Function Generation, E. O. Gilbert (Univ. of Michigan); E Trans. on Electronic Computers, l. EC-8, pp. 391–399; September, 1959.

The design of position and velocity ser- s used in analog computation and simula- n for multiplying and function generation considered. The important characteristics potentiometers, gear train, motor, ampli- r, and tachometer are defined and dis- ssed. Nonlinear performance require- nts, such as velocity and acceleration nits, overshoot for large step inputs, and atic resolution, are defined in terms of com- nent parameters. A minimum gear reduc- n ratio is determined on the basis of ac- leration, frictional torque ratio, overshoot large step inputs, or static resolution. near system analysis is made and related system components and nonlinear per- rmance; in particular, it is shown that atic resolution is limited by servo-amplifier ndwidth for given motor, potentiometers, d gear train. The selection of damping ethods and the reduction of steady-state rors is described. A specific design is con- ered as an example.

5

Transistorized Four-Quadrant Time-Divi- n Multiplier with an Accuracy of 0.1 Per nt, by H. Schmid (Link Aviation, Inc.); E Trans. on Electronic Computers, l. EC-7, pp. 41–47; March, 1958.

A four-quadrant transistorized time division analog multiplier with an over-all accuracy of better than 0.1 per cent of full scale is described. The operation of the circuit is independent of the transistor characteristics, requires no complicated balancing arrangements, exhibits excellent stability, and uses simple, noncritical circuitry. The output voltage is normalized to the same range, between ± 10 volts as the input voltages. The static performance is excellent. A dynamic upper limit of 15 kc is obtained.

B-1: SYSTEMS—THEORETICAL DESIGN

586

A Comparison of Machine Organizations by Their Performance of the Iterative Solution of Linear Equations, by E. J. Gauss (Univ. of California); *J. Assoc. for Computing Mach.*, vol. 6, pp. 476–485; October, 1959.

Different methods of machine organization are compared by testing their performance on a typical problem (matrix inversion by the method of Kaczmarz—a variant of the gradient family of methods). For the purposes of comparison, arithmetic and memory performance are assumed identical. An efficiency scale inversely proportional to the time of solution is devised. With a single address machine assigned the number 1.0, the following numbers are obtained: four-address, 1.25; single-address with index registers, 2.5; complex organization found in the University of Illinois' proposed machine, 9. This machine, with a small ultra-fast memory capable of storing up to 16 commands, and equipped with look-ahead and index facilities, is control-organized to the degree that operation is arithmetic- rather than memory-limited.

587

Some Aspects of the Logical and Circuit Design of a Digital Field Computer, by I. F. Brown (Ferranti Ltd.) and B. Meltzer (Univ. of Edinburgh); *Electronic Engrg.*, vol. 31, pp. 590–592; October, 1959.

The principles of a new type of digital computer for the solution of field problems are described. By making the calculations at all the lattice points of the field simultaneously, computation time is greatly reduced. A unitary (abacus) rather than binary or decimal arithmetic is used. The computation is done by lattice units, one associated with each lattice point of the field. The synthesis of lattice units from simpler basic units is described. The experimental design of a basic unit suitable for potential and other problems is presented and some problems associated with the computer are briefly discussed.

588

Optical Analog Computers, by B. J. Howell (Sperry Rand Corp.); *J. Opt. Soc. Amer.*, vol. 49, pp. 1012–1021; October, 1959.

Certain applications of optical devices in digital computers are described and a general theory of optical analog computers is developed. Certain characteristics of the photographic process make it possible to perform mathematical operations with photosensitive materials, as well as with photocells. These characteristics are: 1) the modulation of light intensities by optically dense films; 2) the addition of densities of superimposed layers; 3) the multiplication of transparencies of superimposed layers; 4) the ability of the photographic emulsion to integrate exposures occurring throughout time or from several sources. Examples of optical methods of calculation are described and the construction of an optical analog computer for synthesizing the two-dimensional Fourier transform of a function for use in crystal structure determination is described. A new machine giving immediate presentation of the results of two-dimensional Fourier transforms is proposed.

B-2: SYSTEMS—DESCRIPTIONS

589

The Univac Air Lines Reservations System: A Special-Purpose Application of a General-Purpose Computer, by D. K. Sampson (Telex, Inc.), V. E. Herzfeld (Remington Rand Univac), and C. W. Fritze (Monarch Electronics Co.); *Proc. Eastern Joint Computer Conf.*, pp. 152–156; December 3–5, 1958.

The application of a Univac File Computer to an airlines reservation system is described. The system services 135 agents with a response time of 1 second for local and 10 seconds for distant inquiries. The problems of message errors, queuing analysis, system expansion, and memory requirements are discussed. Systems servicing up to 1200 agent sets with full-duplex telegraphic communication and no increase in response times are envisaged.

590

The Ferranti-Perseus Data-Processing System, by P. M. Hunt (Ferranti Ltd.); *Computer J.*, vol. 2, pp. 68–75; July, 1959.

The Ferranti-Perseus Data-Processing System, designed specifically for large-scale data handling operations, is described in detail. The memory consists of sixteen word nickel delay lines, each word comprising 72 bits, divided into 12 alpha-numerical characters of 6 bits each. Special features of the machine are the mixed radix arithmetic (particularly suitable for calculations in sterling) and elaborate checking. In addition to the usual parity-bit checking, all arithmetic operations are monitored by a system of check adders. The machine is comparatively slow, with a word time of 234 μsec.

591

PILOT, The NBS Multicomputer System, by A. L. Leiner, W. A. Notz, J. O. Smith, and A. Weinberger (Natl. Bur. of Standards); *Proc. Eastern Joint Computer Conf.*, pp. 71–75; December 3–5, 1958.

The general design features of PILOT, the NBS system of three integrated computers, are described. The primary computer, with special parallel high-speed arithmetic circuits, performs most of the control and arithmetical functions; the secondary computer controls all "housekeeping" operations such as indexing and instruction modification, while the third computer monitors all editing requirements. The computers may modify each others' data and instructions, resulting in a very fast and flexible general purpose system.

592
Design of the RCA 501 System, by J. G. Smith and T. M. Hurewitz (RCA); *Proc. Eastern Joint Computer Conf.*, pp. 160–164; December 3–5, 1958.

The basic features of the RCA all-transistorized 501 Computing System are enumerated. Extremely high reliability results from the standardized solid-state circuits. Failure rates of as low as one transistor failure per 1000 hours of system are claimed. Fast storage is variable word-length magnetic core with a cycle time of 15 μsec, backed by a random access drum file and up to 63 tape units.

593
DART Project, by L. P. Meissner and E. O. Codier (Naval Ordnance Lab.); *U. S. Gov. Res. Repts.*, vol. 32, p. 360(A), September 11, 1959; PB 151 773 (order from OTS $1.50).[1]

DART (Differential Analyzer, Real Time), a computing system that possesses the inherent speed of an analog computer and the basic accuracy of a digital computer, is discussed. Information in two forms, pulse-trains and sets of "static" gating voltages, is processed by a number of digital computing elements of different types which are interconnected in the manner of analog computing elements in order to solve a set of differential equations. The system is described from a mathematical viewpoint, and the construction of the hardware is explained in detail. Some comments concerning inherent errors are made and improvements for future development are suggested.

594
The CORDIC Trigonometric Computing Technique, by J. E. Volder (Convair); IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-8, pp. 330–334; September, 1959.

The trigonometric computing technique utilized in the COordinate Rotation DIgital Computer (CORDIC), a special-purpose digital computer for real-time airborne computation, is discussed. This technique is especially suitable for solving the trigonometric relationships involved in plane coordinate rotation and conversion from rectangular to polar coordinates. CORDIC is an entire-transfer computer; it contains a special serial arithmetic unit consisting of three shift registers, three adder-subtractors, and special interconnections. This special unit is also suitable for other computations such as multiplication, division, and the conversion between binary and mixed radix number systems. (See also Abstract 583.)

595
The Siemens Digital Computer 2002, by H. W. Gumin (Siemens and Halske AG); *Proc. Eastern Joint Computer Conf.*, pp. 157–160; December 3–5, 1958.

The characteristics and construction of the Siemens Digital Computer 2002 are discussed. The transistorized computer is a general purpose decimal machine with a word length of 12 decimals plus sign and an average speed of 2000 operations per second. Special features include three index registers, the use of the instruction location counter for address modifications, automatic address substitution, and fixed- and floating-point operations. The 2002 has a transistor-driven magnetic core memory of variable size (units of 1000, 2500, 5000, and 10,000 words) and a magnetic drum memory with a capacity of 10,000 words. Input and output data are handled by means of punched paper tape and punched cards. Considerable expansion by magnetic tape equipment is possible.

596
The Universal Electronic Digital Machine (URAL) for Engineering Research, by Iu. Ia. Bazilevskii, translated by C. D. Benster (Electrodata Corp.); *J. Assoc. for Computing Mach.*, vol. 4, pp. 511–519; October, 1957.

A general description of the Russian computing machine URAL is given. The machine has 1024 words of drum memory backed by a 40,000-word tape memory and a basic timing of 6000 operations per minute. Operations are single-address and the word length is 36 bits. Arithmetic is done in semiparallel fashion and is comparatively slow (10 msec for addition). The computer is intended primarily for scientific and engineering problems.

597
LEM-1, Small Size General Purpose Digital Computer Using Magnetic (Ferrite Elements), by U. A. Machmudov (A. S. Popov Tech. Soc. of Radio Engrg. and Telecommunications, Moscow), translated by E. M. Zaitzeff (Bendix Syst. Div.); *Commun. Assoc. for Computing Mach.*, vol. 2, pp. 3–9; October, 1959.

The development and construction of LEM-1, a small-scale Russian computer using magnetic core logic and capacitative memory, is described. A section of fast memory attached to the arithmetic unit (which operates in serial-parallel fashion) enables intermediate results to be stored without frequent recourse to the general purpose memory. Reliable operation at temperatures up to 70° C is reported.

598
The High Speed Electronic Calculating Machine of the Academy of Sciences of the U.S.S.R., by Acad. S. A. Lebedev, translated by C. D. Benster (Electrodata Corp.); *J. Assoc. for Computing Mach.*, vol. 3, pp. 129–133; July, 1956.

A general description of the best known Russian computing machine, B.E.S.M., is given. The operative memory is a 1023-word cathode-ray tube memory, backed by a drum and tapes. Instructions are three-address with an average rate of 7000 to 8000 operations per second. Arithmetic, all done in one universal unit, is floating point. Input-output devices are comparatively slow as the computer is intended primarily for mathematical and scientific computations.

599
The Parametron Digital Computer MUSASINO-1, by S. Muroga and K. Takashima (Nippon Teleg. and Tele. Public Corp.); IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-8, pp. 308–316; September, 1959.

Features of MUSASINO-1, a large-scale digital computer with novel logical elements, the parametrons, are described. Primarily designed for scientific use, it does arithmetic operations in parallel, and has fast access memory of ferrite cores wit nonrectangular hysteresis curves. The ma chine has been in almost continuous opera tion since the spring of 1957 and mainte nance experience has indicated that it has a extreme degree of stability and a low inci dence of faults.

600
System Organization of a Multiple-Cockpi Digital Operational Flight Trainer, by H. J Gray, Jr. and A. L. Vivatson (Univ. of Penn sylvania), and H. H. Nishino (RCA); IRI TRANS. ON ELECTRONIC COMPUTERS, vo EC-8, pp. 326–330; September, 1959.

The system organization of a digital com puter, the purpose of which is to activat simultaneously more than one cockpit of a operational flight trainer, is described. Th simulated aircraft are assumed to be all o the same type, but each is simulated inde pendently. The computer is drum-sequence and represents an application of the theor of multiple computers, since there are sev eral different kinds of memories and mor than one arithmetic unit in the system.

B-4: SYSTEMS—TESTING

601
The Athena Computer, A Reliability Report by L. W. Reid and G. A. Raymond (Rem ington Rand Univac); *Proc. Eastern Join Computer Conf.*, pp. 20–24; December 3–5 1958.

The high performance reliability whicl has been achieved in the Remington Ran Univac Athena Guidance Computer is dis cussed. The Athena computer is a large scale general-purpose transistorized digita computer which is part of the Radio Inertia Guidance System for the Titan missile Three Athena computers have been oper ated for 6361 hours with only 27 failures This high reliability results in an unusua maintenance problem in that service peopl have little opportunity to obtain mainte nance experience. To overcome this difficulty chassis which are similar to those in the com puter and in which troubles can be simu lated are now used on a regular basis at eac operational site. The nature of the failure which have occurred and the design philos ophy for a reliable computer are discussed

C-2: AUTOMATA—ARTIFICIAL

602
Imitation of Pattern Recognition and Trial-and-Error Learning in a Conditional Prob ability Computer, by A. M. Uttley (Natl Physical Lab., England); *Rev. Mod. Phys.* vol. 31, pp. 546–548; April, 1959.

The principle of a system developed a the National Physical Laboratory which ca "recognize" patterns and "learn" by tria and error is described. It is pointed out tha in order for a machine to simulate patter recognition and learning, it must be able to a) distinguish sets of signals through the us of coincidence counting; b) recognize tim patterns by use of delay circuits; c) coun occurrences of signals and sets of signals d) store information regarding past occur rences, at least for a certain length of time

il e) calculate ratios to determine relative tes of units with stored counts of occurces.

3

the Mechanical Simulation of Habitrming and Learning, by S. Gorn (Univ. Pennsylvania); *Infor. and Control*, vol. 2, 226–259; September, 1959.

Digital techniques for the simulation of bit-forming and learning are discussed. pes of simulation mechanisms are classiid and types of habit-forming and learning be simulated are discussed, attention be- focussed upon reinforcement. The lanage of computer programming is used to scribe the flow of control and the language mathematical probability is used to anze the effect of various reinforcement nctions on the asymptotic behavior of nulating programs. It is shown, also, in ogramming terms, how the "delay random ector" part of the simulating process may "factored out" as a separate unit applible either to habit-forming or learning, ich latter are distinguished by whether e reinforcements are applied immediately upon "comparison with a goal." Several nforcement models are considered.

4

astic Neurons as Memory Elements, D. G. Willis (Lockheed Aircraft Corp.); 59 IRE WESCON Convention Record, 4, pp. 55–65.

Studies of the logical elements, neurons, the human brain carried out in order to nstruct machines capable of "pattern cognition" or "learning" are discussed. A ass of plastic neuron models is defined, eir information storage capacity is deterined, and the mechanism by which informaon can be read into and out of a system of ch neurons on a random access basis is dertibed. The read-in–read-out properties of a stem of 288 plastic neurons has been simuted on a digital computer. An expression r the output of a plastic neuron as a funcon of its previous history is derived.

D-1: PROGRAMS—AUTOMATIC PROGRAMMING, DIGITAL COMPUTERS

05

n Algebraic Translator, by H. Kanner Univ. of Chicago); *Commun. Assoc. for omputing Mach.*, vol. 2, pp. 19–22; October, 959.

An algebraic translator similar to that roposed by Wegstein [abstract 318] is dertibed. Provision is made for all the comon algebraic manipulations. Exponentiaon, multiplication and addition are perrmed in the stated order, except where herwise dictated by parenthesis, and a stematic flow-chart notation is developed. he translator is in standard 3-address rm. Further syntactic manipulation is reuired for computers of differing address ructure.

05

ALE, A Simple Algebraic Language for Enneers, by W. R. Brittenham, G. Kuss and . Thompson (A. O. Smith Corp.); *Commun. ssoc. for Computing Mach.*, vol. 2, pp. 22–4; October, 1959.

A specialized automatic coding system, tailored to small problems, which fulfills the requirements of simplicity, minimal computer conversion time, and immediate availability of printed results is described. Fast assembly time is achieved by the sharing of memory by the compiler and the compiled program. The object program uses very high precision fixed point arithmetic, partly to avoid scaling problems and partly to provide analysis facilities for larger programs.

607

Proposal for a Feasible Programming System, by P. R. Bagley (M.I.T. Lincoln Lab.); *Commun. Assoc. for Computing Mach.*, vol. 2, pp. 7–10; August, 1959.

The development of a programming facility, itself involving a computer and a program, to assist in the preparation of large-scale real-time programs is outlined. The facility, which will be capable of preparing programs for a large class of machines of similar characteristics, will stress the discovery of errors in source programs, rules of procedure or flow diagrams before the construction of an object program is attempted. A program interrupt scheme, a large set of print-out characters, large random-access storage, and indirect addressing, are among the computer characteristics advocated.

608

IBM 709 Tape Matrix Compiler, by S. D. Hornick (Douglas Aircraft Co.); *Commun. Assoc. for Computing Mach.*, vol. 2, pp. 31–32; September, 1959.

A tape compiler that does all the necessary bookkeeping for the commoner matrix operations is described. The matrices to be operated on are numbered and details of operation on and location of the matrices on tape are entered on punched cards. The program from this point is completely under the control of the compiler. Systems of up to 50 equations can be handled. Operations available include add, subtract, multiply, transpose, invert, and scalar multiplication and division.

609

A Translation Routine for the DEUCE Computer, by R. C. Brigham and C. G. Bell (New South Wales Univ. of Tech.); *Computer J.*, vol. 2, pp. 76–84; July, 1959.

An instruction translation routine called SODA (Symbolic Optimum Deuce Program) for use with the DEUCE computer is described. SODA effectively allows DEUCE to be considered as a three-address machine. Besides incorporating many features peculiar to the machine, it has many features commonly associated with translators such as symbolic addressing, index registers, and a trace routine.

610

Algorithms for Formula Translation, by J. P. Cleave (The University, Southampton); *Computer J.*, vol. 2, pp. 53–54; July, 1959.

An entirely formal method of constructing a program for the evaluation of an implicitly defined quantity is considered. The formal algebra can be programmed and so incorporated in an autocode wherein each step is a line of three-address coding. The method can be expanded to certain systems of implicit equations and thence to the automatic solution of ordinary differential equations.

611

Remarks on ALGOL and Symbol Manipulation, by J. Green, R. M. Shapiro, F. R. Helt, Jr., R. G. Franciotti and E. H. Theil (IBM Corp.); *Commun. Assoc. for Computing Mach.*, vol. 2, pp. 25–27; September, 1959.

Modifications to the ALGOL language suggested by experience gained in constructing an experimental ALGOL processor for the IBM 709 are proposed. The modifications are intended to clarify certain ambiguities in the "for," "if," and "do" statements. Further symbol manipulation additions are also considered advantages.

612

Intercode, A Simplified Coding System for AMOS, by F. J. Berry (British Ministry of Supply); *Computer J.*, vol. 2, pp. 55–58; July, 1959.

Intercode, a special purpose autocode for the use of a Ferranti Mark I machine called AMOS with small scientific-type problems, is described. Simple and easy to learn, it provides three-address programming for an essentially one-address machine. Numbers are stored in floating point, and error diagnosis is provided by monitoring the progress of the calculation by check-printing. Subroutines for various mathematical functions may be called by putting the number corresponding to the function in the A-address and its argument in the B-address. The value of the function will then be placed in the C-address.

D-2: PROGRAMS—APPLICATIONS, DIGITAL COMPUTERS

613

Where Next? Some Conjectures on the Future of the Large-Scale Computer in Integrated Commercial Work, by G. Cuttle (Internatl. Computers and Tabulators Ltd.); *Computer J.*, vol. 2, pp. 85–86; July, 1959.

Means of eliminating the present day plethora of updating and merging operations in data-processing and of creating a smoother over-all operation are discussed. Larger random access memories, parallel programming and machine time sharing are listed as the likely areas of advancement.

614

A Monte Carlo Simulation of a Production Planning Problem, by F. I. Musk (Courtlands Ltd.); *Computer J.*, vol. 2, pp. 80–94; July, 1959.

A computer program which simulates by Monte Carlo techniques the allocation of orders to a set of processing machines is described. The necessary pseudo-random numbers are generated by a multiplicative congruential method. Customer orders from a population of known distribution are classified by a set of priority rules and the program allocates the orders to give the machines the longest possible runs, subject to the priority restrictions. The effects of policy changes may be calculated in terms of idle machine time and delay of completion of orders.

615
An Electronic Directory for Sorting Mail, by A. W. Holt (Rabinow Engrg. Co., Inc.); *Proc. Eastern Joint Computer Conf.*, pp. 79–90; December 3–5, 1958.

The mechanization of mail sorting is discussed. Sorting techniques and the basic directory problems associated with the automatic sorting of mail are described. Directories which utilize magnetic drums or other memory systems are described and evaluated.

616
Automatic Linkage of Vital Records, by H. B. Newcombe, J. M. Kennedy, and A. P. James (Atomic Energy of Canada Ltd.) and S. J. Axford (Dominion Bur. of Statistics, Ottawa); *Science*, vol. 130, pp. 954–959; October 16, 1959.

The use of the Datatron 205 Computer to automatically link the records of births which occurred in the Canadian province of British Columbia during 1955 with the records of marriages which took place in the province during the period 1946–1955 is discussed. To reduce the number of marriage records which the computer must compare with a birth record, use was made of pairs of the parents' surnames. These names were coded (by the computer) in the Russel Soundex Code, a phonetic code consisting of the first letter of the name followed by three numeric digits. The pairing of surnames made the record-matching more efficient than if only single surnames were used. To make a decision the computer also utilizes additional data. The logic operation of the computer, the reliability of the linkages, and the speed of record linkage are discussed. The techniques outlined can be applied to to record matching operations other than marriage and birth records. It is pointed out that a computer which can accept alphabetic information will reduce the time necessary to match records.

617
Digital Computer Programs in Electric Utilities, by R. W. Long, R. T. Byerly, and L. J. Rindt (Westinghouse Electric Corp.); *Electrical Engrg.*, vol. 78, pp. 912–916; September, 1959.

Recently-developed digital computer programs for the solution of electric utility problems concerned with load flow, short circuit, and transient stability studies and with the economic dispatch of system generation and the development of power system loss formulas are briefly described. Such problems can be solved, on a mail order basis, on the IBM 704 computer at Westinghouse.

618
An Application of Digital Computation to a Problem of Army Tactics, by J. Brick (W. L. Maxson Corp.); 1959 IRE WESCON Convention Record, pt. 5, pp. 8–25.

The use of digital computers in the planning of field artillery fire on the divisional level is discussed. The general principles of fire planning are given and information flow diagrams of the computer operations which implement these principles are described. An artillery fire planning program which has been written for a Bendix G-15 D computer is discussed. It is pointed out that the major problems in applying computers to this application are man-machine communication and making the computer behave more like a human fire planner.

619
Non-Symmetric Correlation Matrix Program for the IBM Type 650, by A. Dvorak and C. E. Wright (Washington Univ.); *U. S. Gov. Res. Repts.*, vol. 32, p. 360(A), September 11, 1959; PB 139 636 (order from LC mi $1.80, ph. $1.80).[1]

A program for the IBM 650 computer which will compute nonsymmetric correlation coefficient matrices up to order 20 by 40 with the means, standard deviations, and variances for all the variables is described. All the correlation coefficients are in four decimals, the variances in four decimals more than the input, and the means and standard deviations in three decimals more than the input.

620
Calculation of Gamma Function to High Accuracy, by M. E. Sherry and S. Fulda (A.F. Cambridge Res. Center); *Math. Tables and Other Aids to Computation*, vol. 13, pp. 314–315; October, 1959.

The calculation, to 35 decimal places, of the constants $\Gamma(1/3)$ and $\Gamma(2/3)$ on the Cambridge Computer is discussed. An interpretive routine that treats floating-point numbers of 37 significant digits was employed. Round-off and truncation errors were examined at each step in the calculation. The final relative error was less than $\pm 3 \times 10^{-35}$ in each case.

621
A General Analysis of Variance Scheme Applicable to a Computer with a Very Large Memory, by J. Lieblein (Dept. of the Navy); *J. Assoc. for Computing Mach.*, vol. 6, pp. 469–475; October, 1959.

An efficient means of computing on a high-speed computer with large memory all the sums necessary for a complete r-factor analysis of variance is described. The input data $X_{ij} \cdots$ are assumed stored serially in an unbroken sequence. Expressions for the addresses of memory locations whose contents are to be added when summation is over particular subscripts are derived, and the total number of possible sums and the number of sums when there is summation over at least one subscript are obtained. With the basic sums evaluated, the various analyses of variance formulas are easily applied.

622
Application of a Digital Computer to the Zeeman Method in Atomic Spectroscopy, by K. L. Vander Shreis (Oak Ridge Natl. Lab.); *J. Opt. Soc. Amer.*, vol. 49, pp. 944–947; October, 1959.

The use of high-speed digital computers, and in particular the Oracle Computer, in the classification of atomic spectra is discussed. These computers are useful in this application because of their large capacity memories. The relative merits of three methods for generating possible energy levels or differences of energy levels from available data are examined. It is concluded that the treatment of the observed data in terms of the concept of Zeeman tags is the most useful approach. A specific set of computer routines designed to do both the computational and book-keeping operations of the Zeeman method on the Oracle is described.

623
A Scientific Application of Digital Computers: The 3-Dimensional Structure of the Protein Myoglobin, by J. C. Kendrew (Cavendish Lab., Cambridge); *Computers and Automation*, vol. 8, pp. 10–11; September, 1959.

X-ray crystallographic methods of determining the structure of large protein molecules such as myoglobin and the computations required to obtain the corresponding Fourier coefficients are outlined. It is pointed out that the use of a smaller mesh and faster computation would provide a more accurate picture and thereby would make possible a fuller understanding of the chemical processes in living cells.

624
A General Least-Squares Program for the Refinement of Anisotropic Thermal Parameters, by W. M. MacIntyre (Univ. of Colorado); *Acta Crystallographica*, vol. 12, pp. 761–764; October, 1959.

A program for the refinement of anisotropic thermal parameters and atomic coordinates for any crystal in any space group on the IBM 704 computer is described. The program has been written in two complementary parts, each of which is an independent program. The primary function of the short first program is to calculate the scattering factor for each element and each plane being considered. The second program, which carries out the refinement, is designed to be as flexible as possible. It can be used simply to calculate structure factors. Atomic coordinates and thermal parameters may be refined separately or simultaneously. Provision is made for excluding the atomic coordinates and/or the thermal parameters of an atom from the refinement. The final atomic coordinates and thermal parameters are punched automatically on cards if further refinement is necessary. To conserve machine time, a modified diagonal approximation is used.

625
Use of a Digital Computer for the Calculation of Aberration Coefficients, by P. W. Ford (Univ. of Tasmania); *J. Opt. Soc. Amer.*, vol. 49, pp. 875–877; September, 1959.

The design and performance of a program for the calculation of aberration coefficients of axially symmetrical optical systems, up to and including the tertiary (seventh order) coefficients, on an English Electric Deuce digital computer are discussed. The program is based on a computing scheme developed for a desk calculating machine.

626
Lens Design by Electronic Digital Computer: II, by M. Nunn and C. G. Wynne [Wray (Optical) Works Ltd.]; *Proc. Phys. Soc.*, vol. 74, pp. 316–329; September, 1959.

The application of the method of Successive Linear Approximation at Maximum Steps (see Abstract 460) to automatic lens

sign on a Ferranti Mark 1* electronic gital computer is discussed. The program described and the results of applying the thod to three design problems are given.

7
enerating Strategies for Continuous Sepa-tion Process, by E. E. Bernard and P. D. ole (Univ. of Leeds); *Computer J.*, vol. 2, . 87–89; July, 1959.

A general method of generating all the stinct designs for continuous separation ocesses in the chemical industry and evalu-ing them for construction and operating sts is described. Mixtures of up to ten dif-rent components may be handled. The stem avoids the hazards associated with nd methods of either missing possible de-gns or creating duplications. The method nsists in evaluating the number of distinct rtitions of the components of the mixture.

8
n Application of a Computer to Wind unnel Design, by S. H. Hollingdale and . M. Barritt (Royal Aircraft Establish-ent); *Computer J.*, vol. 1, pp. 42–47, pril 1958; pp. 64–68, July 1958.

Computer solutions of the aerodynamic sign and automatic control of a large wind nnel are described. For supersonic flows it n be shown that if the wall shape of the zzle is assumed unknown, but the flow is nown on one boundary, the solution of the rodynamic equations can proceed in a rogressive manner in both subsonic and personic sections. The equations are trans-rmed to avoid the usual singularities at lach One, yielding a set of computed wall apes that can be changed smoothly and ntinuously over a range of sub- and super-nic operating conditions.

29
imulation of Transistor Switching Circuits n the IBM 704, by R. J. Domenico (IBM orp.); IRE Trans. on Electronic Com-uters, vol. EC-6, pp. 242–247; December, 957.

Given the configuration and the equiva-nt representation of the transistors in a witching circuit, a computer program yield-ng the performance of the circuit and the ean value of its parameters is described. he transistor nonlinearity is handled by iecewise linearization of an equivalent cir-uit. Rules to combine this procedure ef-ciently with the matrix manipulation of the near external circuitry are provided. The ethod can be extended to combinations of asic circuits containing up to ten transis-ors.

30
alculation of Transient Stability Problems sing a High-Speed Digital Computer, by . W. Stagg, A. F. Gabrielle, D. R. Moore, nd J. F. Hohenstein (Amer. Elec. Power ervice Corp.); *Power Apparatus and Sys-ems*, no. 43 (*AIEE Transactions*, pt. III, ol. 78), pp. 566–574; August, 1959.

The development and application of an BM 704 program for the solution of tran-ent stability problems involving both in-uction and synchronous machines is de-cribed. The stability problems can be olved without the need of a network ana-zer for such supplementary measurements as admittance constants, initial machine voltage, and slips. The program can represent a total of 50 induction and/or synchronous machines, 200 busses, and 300 lines and/or transformers, and simulates automatically a desired sequence of fault conditions and switching operations. Any number of machines, including combinations of synchronous and induction motors or generators, can be represented on any single bus. The program provides a tabulation of all system and machine voltages, machine currents, accelerating torques and slips at each time interval and, in addition, plots swing curves (slip vs time) of synchronous and induction machines for quick analysis during the calculations. The nodal iterative method for the solution of system voltages and currents is combined with Gill's variation of the Runge-Kutta procedure for the solution of the differential equations describing synchronous and induction machine behavior. The nodal method permits the identity of the system to be retained, and thereby provides access to system voltages and currents during transient disturbances.

631
Iteration Methods for Digital Load Flow Studies, by J. E. Van Ness (Northwestern Univ.); *Power Apparatus and Systems*, no. 43 (*AIEE Transactions*, pt. III, vol. 78), pp. 583–588; August, 1959.

The convergence of the solution of an electrical power flow problem solved by iteration techniques on a digital computer is discussed. Two sets of equations are considered, the original set of nonlinear equations and variational equations formed from the equations for the total differentials of the variables. The second set is linear and may be handled by any of the methods generally used for solving sets of linear equations. The solutions of the second set are then used as correcting factors in the first set, and by proceeding back and forth, a solution is obtained. Various methods of doing this are considered; one method essentially cuts in half the number of iterations needed for a solution. The use of this method of analysis, together with acceleration methods such as those suggested by Brown and Tinney, may result in even faster convergence of the system.

632
A Reactor Code for the Narec, by S. Podgor and L. A. Beach (Naval Res. Lab.); *U. S. Gov. Res. Repts.*, vol. 32, p. 360(A), September 11, 1959; PB 139 727 (order from LC mi $2.40, ph $3.30).[1]

A few-group, multiregion, one-dimensional reactor code which has been prepared for the Naval Research Laboratory Electronic Digital Computer (Narec) is discussed. The code applies to slab, cylindrical, and spherical geometries. For any geometry and material composition, the calculation gives a) the multiplication constant, b) the spatial flux distribution for each energy group, and c) the spatial source distribution. Calculations of two critical arrangements of the Naval Research Reactor are described. Comparison of calculated and experimental results indicates that they are within five per cent of each other or better.

633
The Solution of Railway Problems on a Digital Computer, by A. Gilmour (The English Electric Co., Ltd.); *Computer J.*, vol. 1, pp. 25–28, April 1958; pp. 78–83, July, 1958.

The analysis and solution of typical railroad problems on the DEUCE calculator are described. Engineering and design applications include electric motor and rectifier design, locomotive performance under certain restrictions, and power supply loading produced by an ac traction network. Examples of operational problems include the calculation of point-to-point running times, the preparation of timetables, and linear programming optimization of empty car movements.

634
Computational Aspects of Brain Function, by R. G. Bickford (Mayo Clinic and Mayo Foundation); IRE Trans. on Medical Electronics, vol. ME-6, pp. 164–167; September, 1959.

The application of computers to the study of the brain is discussed. The difficulties involved in this particular application are pointed out, *viz.*, the errors introduced by the coupling between the organisms and the recording instrument or between the organism and a transducer; the lack of knowledge concerning common brain rhythms; the difficulty in isolating systems; the presentation of data in such a way as to prevent proper interpretation; and the need for continuous immediate presentation of the data. Some systems in which computers have been successfully employed are briefly described.

635
Digital Recording of Electrocardiographic Data for Analysis by a Digital Computer, by L. Taback, E. Marden, and H. L. Mason (Natl. Bur. of Standards) and H. V. Pipberger (Veterans' Admin. Hospital and Georgetown Univ. School of Medicine); IRE Trans. on Medical Electronics, vol. ME-6, pp. 167–171; September, 1959.

The analysis of electrocardiographic (ECG) data on an IBM 704 digital computer is discussed. The data is recorded initially on three channels of a four-channel magnetic tape. The techniques employed to convert one or more of the cardiac cycles to digital data are described. Since the data is not prepared under the control of the 704 test programs have been written to check whether the information contained on the tape is compatible with the 704. The method by which the computer determines the beginning of the *P* wave is described. Punched cards containing additional information about a patient and the same identification number as the digital tape containing his electrocardiogram can be fed into the computer together with the tape in order to make correlations of various factors among groups of patients.

636
Desk Calculator Determinations of Human Dynamics, by E. S. Krendel and H. L. Platzer (Franklin Inst.); *U. S. Gov. Res. Repts.*, vol. 32, p. 359(A), September 11, 1959; PB 137 316 (order from LC mi $2.70, ph $4.80).[1]

The possibility of computing describing functions and remnants for the study of human dynamics with relatively cheap digital equipment is discussed. Procedural aids which simplify the hand calculation checkout of complex computing programs intended for high-speed digital machines are given. The selection of the sampling interval on the basis of the transport delay of the system as well as the Shannon sampling theorem is discussed and representative computations for a specific example are presented.

637
Statistical Programs for the IBM 650, by J. W. Hamblen (Univ. of Kentucky); *Commun. Assoc. for Computing Mach.*, vol. 2, pp. 13–18, August, 1959; pp. 32–37, October, 1959.

Brief descriptions of statistical programs available on IBM 650 computers in university computing centers are given. The programs are grouped under the headings: Experimental Design, Correlation, Multiple Regression, Factor Analysis, Curve and Surface Fitting, Time Series, Biserial Correlation, Frequency Tabulations, Chi Square, Phi Coefficients, etc., and Random Numbers.

638
On a Problem of Network Topology, by T. Fujisawa (Univ. of Oskaka Prefecture); IRE TRANS. ON CIRCUIT THEORY, vol. CT-6, pp. 261–266; September, 1959.

A method for obtaining all possible trees or cotrees and signs of cotree determinants, which are necessary in mesh basis analysis of networks with mutual and active elements, is described. Computations are based on fundamental circuit matrices. A transformation from one tree to another tree may be performed by elementary transformations on circuit matrices. By this method, all the trees and fundamental circuit matrices may be determined. Signs of cotree determinants and their minor determinants of a fundamental circuit matrix also may be easily determined. The method is suitable for use on digital computers.

639
A Method for the Solution of the *N*th Best Path Problem, by W. Hoffman and R. Pavley (Wayne State Univ.); *J. Assoc. for Computing Mach.*, vol. 6, pp. 506–514; October, 1959.

A method for the computation of the *N*th best path through a network whose links are weighted with a value is described. The method is an extension of and depends on the minimum tree method of finding the best path. The minimum tree is first evaluated and deviations from it are computed to order other possible paths according to their value. The problem has application in the control of street traffic.

640
Formal Procedures for Connecting Terminals with a Minimum Total Length of Wire, by H. Loberman and A. Weinberger (Nat. Bur. of Standards); *J. Assoc. for Computing Mach.*, vol. 4, pp. 428–437; October, 1957.

Total wire length minimization is important in a high-speed digital computer in order to reduce the capacitance and delay line effects of long leads. Two procedures, together with flow diagrams each of which leads to the minimum tree solution to the problem, are given. The procedures differ according to the manner in which the branches between terminals are sorted.

641
Digital Information Process for Machine-Tool Control, by A. K. Susskind (M.I.T.); IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-7, pp. 136–140; June, 1958.

A digital system for the control of a milling machine is described. Given the contour specifications of the piece to be cut, the computer determines straight-line paths, approximating the contour within the desired accuracy, and calculates the cutter-center path corresponding to the straight lines. From this a tape providing complete control over the milling machine motions is prepared. Further utilization of the computer to participate in the initial design as well as the cutting of the part is indicated.

642
Organization and Retrieval of Records Generated in a Large-Scale Engineering Project, by G. A. Barnard III (Stanford Res. Inst.) and L. Fein; *Proc. Eastern Joint Computer Conf.*, pp. 59–63; December 3–5, 1958.

A multicoordinate system for filing and retrieving all the documents connected with a large-scale engineering project is described. The system is discussed in connection with the development of a large-scale computer and data processing system but is also applicable to other technical projects. Records are filed in folders under system categories by means of a numeric code and under category attributes by means of an alpha-numeric code. It was originally intended to make the file a three-dimensional one by filing documents also by the user of the information contained in them. This, however, was abandoned due to the expense involved. The file system is both closed and expandable.

643
The Trial Translator, An Automatic Programming System for Experimental Russian-English Machine Translation, by V. E. Guiliano (Harvard Univ.); *Proc. Eastern Joint Computer Conf.*, pp. 138–144; December 3–5, 1958.

An automatic programming system, the Trial Translator, for the automatic testing of translation algorithms, the grammatical and syntactic rules for the production of smooth automatic translations between human languages, is discussed. The automatic translation of Russian to English is considered. The system accepts as its inputs a set of experimental translation algorithms expressed in a suitable pseudocode language and a Russian technical text. The system applies the algorithms to the text and produces, as its output, a readable trial translation. The Trial Translator contains three main subsystems, the Automatic Dictionary, the Formula Inserter (a compiler program) and a Specifier-Evaluator-Editor (an interpretive program).

644
Pattern Detection and Recognition, by S. H. Unger (Bell Tel. Labs., Inc.); PROC. IRE, vol. 47, pp. 1737–1752; October, 1959.

Two types of pattern-processing problems are discussed. The first, termed "pattern detection," consists of examining an arbitrary set of figures and selecting those having some specified form. The second problem, "pattern recognition," consists of identifying a given figure which is known to belong to one of a finite set of classes. This is the problem encountered when reading alpha-numeric characters. Both recognition and detection have been successfully carried out on an IBM 704 computer which was programmed to simulate a spatial computer (a stored-program machine comprised of a master control unit directing a network of logical modules). One of the programs tested consisted of a recognition process for reading hand-lettered sans-serif alpha-numeric characters. This process permits large variations in the size, shape, and proportions of the input figures and can tolerate random noise when it is well scattered in small specks. Programs for detecting L-shaped (or A-shaped) figures in the presence of other randomly drawn patterns have also been successfully tested.

D-3: PROGRAMS—TECHNIQUES, DIGITAL COMPUTERS

645
Parallel Programming, by S. Gill (Ferranti Ltd.); *Computer J.*, vol. 1, pp. 2–10; April, 1958.

As computers become faster, the idle time caused by the comparative slowness of peripheral devices becomes increasingly objectionable. Parallel programming, *i.e.*, the assignment of priorities to the various operations under the control of the computer so as to enable the rest of the computer to continue with useful work while one piece of equipment is tied up with a slow operation, is presented as a solution to the problem. The advantages cited include the elimination of conventional storage, the simultaneous operation of a production program and a program to be debugged, and parallel operation of realtime control applications or information look-up, with routine calculations. It is concluded that the resulting increased complexity of programming will not present insuperable problems.

646
A Proposal for a Generalized Card Code for 256 Characters, by R. W. Bemer (IBM Corp.); *Comm. Assoc. for Computing Mach.*, vol. 2, pp. 19–24; September, 1959.

A proposal for expanding the present highly redundant punched card code to include, for example, all the International Algebraic Language Symbols is discussed. Such an expansion must be compatible with the existing code, contain at least 256 new characters and be further expansible, be reproducible on existing key punches, and have one-to-one correspondence between character and code. A solution satisfying these criteria and having no more than four punches per column is developed.

647
On the Construction of Micro-Flowcharts, by S. Gorn, P. Z. Ingerman, and J. B. Crozier (Univ. of Pennsylvania); *Commun. Assoc. for Computing Mach.*, vol. 2, pp. 27–31; October, 1959.

The construction of Micro-Flowcharts scribing the operation of individual ter instructions is advocated and a sys- matic method of accomplishing this trans- ion is presented. By these means the simu- ion of one machine upon another and the oper choice from available machines of the e most suited to a particular application ll be facilitated.

8
mpirical Test of an Additive Random umber Generator, by B. F. Green, Jr., E. K. Smith, and L. Klem (MIT Lincoln ab.); *J. Assoc. for Computing Mach.*, vol. 6, o. 527–537; October, 1959.

The experimental testing of the appar- t randomness of numbers generated the additive congruential process $X_j=(X_{j-1}+X_{j-n})$ mod 1 where the X's are ositive fractions is described. Frequency, Poker," serial correlation and run length stribution tests were performed. The umbers were satisfactory except for a non- ndomness in runs for $n\leq 16$ which can be moved by discarding alternate numbers. he process has the advantage compared ith multiplicative processes that addition much faster than multiplication on many achines.

49
he Principles of Sorting, by D. A. Bell Jniv. of Birmingham); *Computer J.*, vol. pp. 71–77; July, 1958.

The amount of storage and the number operations required by the better-known ethods of sorting such as pigeon-hole, dix, merging, repeated comparisons, in- rtion, address calculation, selection, and ounting are compared and general princi- es that help to determine which methods combination of methods is most suitable r a particular application on a given com- uter are enunciated.

50
orting on Electronic Computers, by E. H. riend (N. Y. Life Ins. Co.); *J. Assoc. for omputing Mach.*, vol. 3, pp. 134–168; July, 956.

A complete synopsis of all aspects of the rocess of sorting is provided. All the better nown sorting methods such as internal erging, inserting, exchanging, radix sorting ounting, and selecting are described. Opti- um methods of attack for multitape sorts re discussed. Estimates of machine-time nd number of operations for each of the ajor methods are provided.

51
orting by Address Calculation, by E. J. saac and R. C. Singleton (Stanford Res. nst.); *J. Assoc. for Computing Mach.*, vol. 4, p. 169–174; July, 1956.

Sorting of items by calculation of an ad- ress function is described. Usually only a tatistical approximation to the address unction is known. If the approximation is ell chosen, sorting time approaches the igeon-hole method; a bad choice reduces he time of that of the file insertion method. or sorting random numbers, the optimal hoice (established empirically) is to have a traight line address function with successive items 2.4 units apart. Estimates indicate that for random numbers this method is more than twice as fast as conventional merge-sort methods.

652
Amphisbaenic Sorting, by H. Nagler (IBM Corp.); *J. Assoc. for Computing Mach.*, vol. 6, pp. 459–468; October, 1959.

A method of sorting data that requires only $p+1$ tape drives, where the key is expressed in the radix p, is described. The unsorted data is stored initially on the $(p+1)$st tape. An iterative scheme of splitting blocks of data whose designation has the highest numerical value into p partitions according to the most significant digit of the designation produces finally the completely sorted data on tape $(p+1)$. By reading tapes in one and writing in the reverse direction, any group required for splitting is always under the head of the appropriate tape unit; and the final positions of the tapes are the same as their initial positions. When the size of a group permits, it is sorted to completion internally instead of being distributed over the tapes. Convenient algorithms for encoding and decoding the key numbers from any radix into radix p are given.

653
The Influence of Storage Access Time on Merging Processes in a Computer, by P. F. Windley (Univ. of Leads); *Computer J.*, vol. 2, pp. 49–53; July, 1959.

A detailed analysis of the influence of internal storage access time on the optimum number of strings for a merging process is presented. Optimum sizes of blocks for transfer are computed, with particular reference to the Ferranti Pegasus computer. Built-in instructions capable of selecting the largest of three or more numbers are suggested for future data-processing computers.

D-5: PROGRAMS—APPLICATIONS, ANALOG COMPUTERS

654
Operational Analog Simulation of the Vibration of a Beam and a Rectangular Multicellular Structure, by A. B. Clymer (North Amer. Aviation, Inc.); IRE TRANS. ON ELECTRONICS, vol. EC-8, pp. 381–391; September, 1959.

The use of an operational analog computer for the solution of structural problems is discussed. A beam problem and a rectangular multicellular structure problem were run to test the method. It is shown that the method is highly competitive with digital computer and passive-element computer methods for solution of any structural problem.

655
Analog Computer Aids Heart Ailment Diagnosis, by R. L. Skinner and D. K. Gehmlich (Esco, Inc.); *Electronics*, vol. 32, pp. 56–59; October 2, 1959.

An analog computer which measures the rate of flow of blood from the heart is described. A dye is injected into the venous side of the heart and the concentration of the dye in the blood stream is measured as a function of time at the exit of the heart. Tape recordings of the dye curve are used as the input to the computer. The exponent corresponding to the exponential decay of the true dye curve before recirculation begins is determined. An exponentially decaying function which has the same exponent and the same initial value as that of the original dye curve decay is generated. When the decay of the original dye curve remains exponential for a given time and before recirculation begins, the generated function replaces the actual dye curve. The blood flow rate is measured by integrating the area under the actual dye curve and under the generated curve when it replaces the actual curve.

656
A Statistical Study of the Effects of Electric Fields on the Movements of Mammalian Sperm Cells, by J. W. Trank (Univ. of Minnesota); IRE TRANS. ON MEDICAL ELECTRONICS, vol. ME-6, pp. 174–179; September, 1959.

The development of a microtechnique to facilitate the study of electric field effects on the swimming pattern of sperm cells is discussed. The instrumentation for this technique, a microelectrophoresis vessel, a metering motion picture projector, and a simple analog computer for data handling, are briefly described.

E-1: MATHEMATICS—LOGIC—THEORETICAL MATHEMATICS

657
On the Reduction of Continuous Problems to Discrete Form, by J. Greenstadt (IBM Corp.); *IBM J. Res. & Dev.*, vol. 3, pp. 355–363; October, 1959.

The reduction of a continuous problem, defined as one involving derivatives or integrals, to a discrete problem, involving only algebraic or evaluative operations, is discussed. An approach involving cells instead of points is taken, and the unknown function is approximated by functional representations, each associated with one cell and an associated set of parameters. Suitable operations, each associated with a particular cell, are then defined. These operations remove the configuration coordinates from the problem, leaving only the parameters. Similar operations which link the approximations in adjacent cells and which translate certain interface conditions to relations between parameters associated with cells are defined. The entire set of relations is then the equivalent of the usual difference equations. A variational algorithm is introduced in order to circumvent certain difficulties associated with matching equations and unknowns. This also permits the convenient retention of certain "exact conditions" associated with the continuous problem. Some illustrative examples are given.

E-2: MATHEMATICS—LOGIC—SYMBOLIC LOGIC, BOOLEAN ALGEBRA, NUMBER SYSTEMS

658
The Philosophy of Automatic Error Correction, by R. M. Block (Minneapolis-Honeywell Regulator Co.); *Proc. Eastern Joint Computer Conf.*, pp. 25–28; December 3–5, 1958.

Following a discussion of the inherent weaknesses of the theoretical design of error detecting and correction systems, the empirical design of such systems is discussed. Two classes of error correction, "reversion" and "deductive," and an automatic error correction system, Orthotronic Control, are described.

659
An Idealized Over-All Error-Correcting Digital Computer Having Only an Error-Detecting Combinational Part, by W. L. Kilmer (Montana State College); IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-8, pp. 312–325; September, 1959.

The block diagram of an idealized over-all error-correcting digital computer is presented. This computer has the property that during each unit time interval it can correct the effects of a specific maximum number of transient-type component failures which might occur anywhere within it. Yet, all its combinational logic circuitry is only of the error-detecting type. The corresponding reduction in equipment that this design feature makes possible is achieved at the expense of the computer's having to sit idle during a large percentage of those time intervals in which component failures occur. In a sense, therefore, the computer utilizes a great deal of time-domain redundancy as well as equipment-domain redundancy. Some of the design requirements that are involved in using this type of redundancy structure are discussed.

660
A Note on Error Detection in Noisy Logical Computers, by M. Eden (M.I.T.); *Infor. and Control*, vol. 2, pp. 310–313; September, 1959.

A method of error detection for noisy logical computer elements is proposed. The proposal extends the range of the propositional variables so that residue class check symbols may be used in error detection. The principal consequence is that individual logical elements may be designed to process binary inputs with arbitrary reliability and nonzero channel capacity.

661
State-Logic Relations in Autonomous Sequential Networks, by W. H. Kautz (Stanford Res. Inst.); *Proc. Eastern Joint Computer Conf.*, pp. 119–127; December 3–5, 1958.

The synthesis of sequential networks is discussed. The relationship between the internal logic and the state sequential behavior of such networks is examined through the mechanism of a certain mathematical model of the network. In particular, some conditions for the network to be nonsingular, *i.e.*, to have a state diagram which is deterministic even in reversed time, are derived and some important consequences of the nonsingularity condition are demonstrated. The effects on the state diagram of several kinds of constraints imposed on the logic are determined. Several classes of sequential nets are analyzed: the nonlinear feedback shift register, the safe-asynchronous net, the fully self-independent net, and the net with cyclically permuted logic. The realization problem using several types of binary storage elements such as set-reset flip-flops, trigger flip-flops, delay elements, relays, etc., are discussed.

662
Multi-Functional Circuits in Functional Canonical Form, by H. A. Curtis (N.A.S.A.); *J. Assoc. for Computing Mach.*, vol. 6, pp. 538–547; October, 1959.

Fundamental canonical forms derived in an earlier paper (see Abstract 375) are applied to multiple output switching circuits and to the formulation of cost bounds on these circuits. A multi-functional canonical form in the design of single output circuits, based on Shannon's method, is discussed. A gain in efficiency in the multiple output case of at least 20 per cent is demonstrable if the possibility of sharing common subfunctions in taken into account.

663
Minimizing the Number of States in Incompletely Specified Sequential Switching Functions, by M. C. Paull and S. H. Unger (Bell Tel. Labs., Inc.); IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-8, pp. 356–367; September, 1959.

Given a sequential switching function in the form of a flow table in which some of the entries are unspecified, the problem of reducing the number of rows in that flow table is extremely complex, and cannot, in general, be solved by any simple extension of the methods used for completely specified functions. An analysis of the problem is presented, and a partially enumerative solution is evolved. A rough indication of the efficiency of the given procedures may be obtained from the fact that these techniques have been successfully applied to approximately two dozen tables ranging up to about 15 rows. No solution requires more than two hours.

664
The Design and Use of Hazard-Free Switching Networks, by D. A. Huffman (M.I.T.); *J. Assoc. for Computing Mach.*, vol. 4, pp. 47–62; January, 1957.

The occurrence and prevention of both static and dynamic hazards with particular reference to contact networks is discussed. A hazard-free canonical form of any network is derived and the results are applied to preventing hazards in gate networks and in the synthesis of sequential circuits.

665
Algebraic Topological Methods for the Synthesis of Switching Systems, Part III: Minimization of Nonsingular Boolean Trees, by J. P. Roth and E. G. Wagner (IBM Corp.); *IBM J. Research & Dev.*, vol. 3, pp. 326–344; October, 1959.

An algorithm for solving a general problem in combinational switching circuit minimization theory is given. The circuits considered consist of a disjunction (OR-ing together) of trees of any set of logical elements, with the restriction that in any given tree no input appears more than once. To each logical element is attached a positive cost. A method for designing a minimum-cost circuit of this variety for any given logical function is presented. Two parallel treatments are given, one viewing it as an abstract mathematical problem, the other considering it as an engineering problem.

666
The Synthesis and Analysis of Digital Systems by Boolean Matrices, by J. O. Campeau (Litton Industries); IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-6, pp. 232–241; December, 1957.

Methods whereby Boolean matrices may be used to synthesize digital systems are described. The design procedure may be systematized analogously to the application of matrix methods to electrical circuit design. A Boolean equation model for the minimization of the number of memory flip-flops in a synchronous digital system is presented. The method is also applicable to the problems of optimum logical design and optimal programming.

667
Synthesis of Electronic Circuits for Symmetric Functions, by G. Epstein (Hughes Aircraft Co.); IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-7, pp. 57–60; March, 1958.

A systematic procedure for the synthesis of electronic circuits realizing symmetric Boolean functions is developed, as the Shannon "fold-down" method for relays is not applicable to unilateral electronic devices. A minimal-NOT condition is shown to exist for symmetrical functions. As with the minimal-OR condition, the minimal-NOT circuit does not necessarily imply the most economical realization except for the case of fundamental symmetric functions. Nonetheless, it provides a powerful tool for synthesis.

668
Algebraic Method for Simplification of Boolean Functions, by N. T. Grisamore, L. S. Rotolo, *et al.* (George Washington Univ.), *U. S. Gov. Res. Rept.*, vol. 32, p. 486(A), October 16, 1959; PB 140 989 (order from LC mi $2.40, ph $3.30).[1]

An algebraic process for reducing Boolean Functions having many variables to minimal forms is discussed. The process, which involves an operation on the position numbers of units in the truth value of the function to be reduced, can be computer programmed.

669
Shift-Register Code for Indexing Applications, by M. Nadler and A. Sengupta (Indian Statistical Inst.); *Commun. Assoc. for Computing Mach.*, vol. 2, pp. 42–43; October, 1959.

A ten-bit shift register code for calling 64 telemetering stations in a fixed cyclic order is described. The 64 ten-bit code words identifying the stations are selected to permit single error-correction. Embedding the 64 words in the shift register code with period 1023 permits operation without punctuation. The properties and applications of the code, and the computation of the particular minimum distance three code employed, are described in detail.

670
Analysis of Sequential Machines, by D. D. Aufenkamp (Lockheed Aircraft Corp.) and F. E. Hohn (Univ. of Illinois); IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-6, pp. 276–285; December, 1957.

Starting from Mealy's model of a sequential machine, a connection matrix which completely describes the machine is developed. The equivalence of states of a sequential machine is analyzed systematically by an iterative technique. With equivalence established, the connection matrix for the simplest equivalent machine is simply derived. The method, even in complex cases, is readily programmed for computer execution.

671
Minimal Sequential Machines, by D. B. Netherwood (Wright Air Dev. Center); IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-8, pp. 339–345; September, 1959.

The general class of sequential machines defined by Mealy is investigated. It is found that any such machine can be identified with a set of machines of equivalent minimality. A procedure for developing the aggregate of all sets of gates for such minimal machines is evolved, and the problem of selecting components for constructing machines is discussed.

672
A Technique for the Reduction of a Given Machine to a Minimal-State Machine, by S. Ginsburg (Hughes Res. Labs.); IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-8, pp. 346–355; September, 1959.

A technique for reducing an arbitrary machine S as much as possible to a machine T which can do everything (from the input-output point of view) that S can do is presented. Since the technique is always applicable, it is more powerful (although more cumbersome) than the well-known merging technique. Several examples are given.

E-3: MATHEMATICS—LOGIC NUMERICAL ANALYSIS

673
On the Spectral Norms of Several Iterative Processes, by J. W. Sheldon (Computer Usage Co., Inc.); *J. Assoc. for Computing Mach.*, vol. 6, pp. 494–505; October, 1959.

The spectral norm of a square symmetric positive definite matrix is defined as the positive square root of the maximum magnitude of its characteristic roots. A measure of the effectiveness of an iterative method of matrix inversion is derived in terms of the spectral norm. Various theorems concerning the spectral norm are proved, the results obtained are applied to all the well-known iterative processes and suggestions for improving the rate of convergence of some of these processes are made.

674
Construction of a Set of Test Matrices, by M. J. Aegerter; *Commun. Assoc. for Computing Mach.*, vol. 2, pp. 10–12; August, 1959.

The equations and properties of a set of test matrices suitable for determining the accuracy of routines for finding the inverse, determinant, and eigenvalues of a matrix are developed. The matrices are characterized by an exact inverse. The M-condition numbers of Turing and the P-condition numbers suggested by von Neumann and Goldstine are calculated for the test matrices.

675
The Calculation of the Eigenvectors of Co-Diagonal Matrices, by J. H. Wilkinson (National Physical Lab.); *Computer J.*, vol. 1, pp. 90–96; July, 1958.

The sources of the errors which may arise from the straightforward determination of the eigenvectors of a matrix C in Given's co-diagonal form are analyzed. Unless care is taken in the recursive solution of the simultaneous equations corresponding to the approximation to a particular eigenvalue, catastrophic errors not infrequently result. A remedial suggestion is to equate the system of equations C_x to an arbitrary vector b, whose method of selection gives reasonable confidence that, if it be considered as a linear combination of the eigenvectors of C, it will not be particularly defective in any of them.

676
Multi-Dimensional Least-Squares Polynomial Curve-Fitting, by F. H. Lesh (Calif. Inst. Tech.); *Commun. Assoc. for Computing Mach.*, vol. 2, pp. 20–30; September, 1959.

A compact notation to handle multi-dimensional polynomial least-squares curve-fitting is developed. The analysis proceeds exactly as in the one-dimensional case. A computer program to organize such a calculation is flowcharted.

677
On Taking the Square Root of a Complex Number, by C. Strachey (Natl. Res. Dev. Corp., London); *Computer J.*, vol. 2, p. 89; July, 1959.

A concealed danger, due to cancellation resulting from a subtraction, in taking the square root of a complex number is noted. One solution is to take intermediate square roots to double length accuracy; another is to find the root not affected by the cancellation and to obtain the second root from it.

678
Tshebysheff Approximations for Power Series, by R. C. Minnick (Burroughs Corp.); *J. Assoc. for Computing Mach.*, vol. 4, pp. 487–504; October, 1957.

A variant of the Lanczos technique of Tshebysheff economization of a power series is described. The method does not increase the absolute error within a given range, yet avoids much of the manipulation of the original Lanczos method. A function to predict the approximation error is developed and the method of computation is outlined. Extensive tables of Tshebysheff approximations are supplied.

679
New Formulas for Computing Incomplete Elliptic Integrals of the First and Second Kind, by A. R. DiDonato and A. V. Hershey (U. S. Naval Weapons Lab.); *J. Assoc. for Computing Mach.*, vol. 6, pp. 515–526; October, 1959.

Series expansions for computing incomplete elliptic integrals of the first and second kind for large values of the amplitude and modulus are developed. Classical binomial expansion series may be used for small amplitude and modulus and a criterion for terminating the binomial series is given. Series expansion evaluation of elliptic integrals is compared with the well-established Legendre method depending on the Landen transformation. The series method was found to be more accurate and efficient without sacrificing programming compactness. Details of the program encoded on the NORC machine are given.

E-6: MATHEMATICS—LOGIC—LINEAR PROGRAMMING

680
The Alpha Vector Transformation of a System of Linear Constraints, by S. J. Werson (Burroughs Corp.); *Commun. Assoc. for Computing Mach.*, vol. 2, pp. 33–34; September, 1959.

A vector transformation that minimizes the number of artificial vectors required in the solution of a linear programming problem where all the constraint coefficients are of unit magnitude is described. The transformation allows additional flexibility in manipulating the system before computation

681
On an Application of Dynamic Programming to the Synthesis of Logical Systems, by R. Bellman (The RAND Corp.); *J. Assoc. for Computing Mach.*, vol. 6, pp. 486–493; October, 1959.

The methods of dynamic programming and their applications to the synthesis of logical systems are described. In general terms, an M-dimensional input vector, X, whose components assume only the values 0 or 1 is transferred by n-sequential transformations into an output vector Y. With a deviation metric

$$\| Y - Z \| = \sum_{i=1}^{M} | Y_i - Z_i |$$

defined (where Z is any intermediate vector), the methods of dynamic programming may be applied to determine the minimum number of steps to go from X to Y, or to minimize the deviation from Y if the number of operations is limited. The algorithms of dynamic programming show how to proceed optimally from one stage to the next with the number of computations increasing only linearly with the number of stages considered. The general principles are illustrated by a simple example involving a delay element.

F: PERSONNEL

682
The Role of the University in Computers, Data-Processing, and Related Fields, by L. Fein (Palo Alto); *Commun. Assoc. for Computing Mach.*, vol. 2, pp. 7–14; September, 1959.

Existing university programs in the United States in the fields of computers, data-processing, operations research and related subjects are reviewed. Many present computer activities will develop into full-scale disciplines and as such will be the legitimate sphere of the university scholar. In this light an integrated university program under a separately constituted Graduate School of Computer Sciences is recommended. Details relating to the policies, administration, financing, curricula, faculty and students within such an arrangement are discussed.

683
An Educational Program in Computing, by J. Hollingsworth (Rensselaer Polytech. Inst.); *Commun. Assoc. for Computing Mach.*, vol. 2, p. 6; August, 1959.

An educational program currently being developed at Rensselaer Polytechnic Institute to familiarize all students with numerical methods and computers is described. Students are introduced to differential equations in their sophomore year with a heavy emphasis on numerical methods of solution. Visual methods of instruction, including closed circuit television and automatic grading of student programs is discussed.

G: BIBLIOGRAPHIES

684
Bibliography on Numerical Analysis, by A. S. Householder (Oak Ridge Natl. Lab.); *J. Assoc. for Computing Mach.*, vol. 3, pp. 85–100; April, 1956.

A bibliographical list of 321 books and papers on topics concerning numerical analysis is provided. The list brings up to date a bibliography published as an appendix in the author's "Principles of Numerical Analysis." The emphasis is heavily on papers dealing with matrix algebra.

685
Logical Machine Design—A Selected Bibliography, by D. B. Netherwood (Wright-Patterson AFB); IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-7, pp. 155–18, June, 1958; vol. EC-8, pp. 367–380, September, 1959.

A wide coverage of current bibliographic references on the logical design of machines is provided. A salient feature of the bibliography is the extensive indexing of significant title words. Each indexed word is given in the complete context of the title in which it occurs. A total of 777 references is included.

J: SUMMARIES AND REVIEWS

686
New Logical and Systems Concepts, by R. K. Richards; *Proc. Eastern Joint Computer Conf.*, pp. 51–55; December 3–5, 1958.

Future developments in computer systems technology are discussed. It is pointed out that computers can be designed and built more efficiently than in the past if the technologies of physics, components, circuits, logical design, system design, programming, and manufacturing are effectively combined. For example, circuit design can be greatly simplified by the use of Boolean algebra.

687
Octal Diagrams of Binary Conception and Their Applicability to Computer Design Logic, by Shu-T'ien Li; *Commun. Assoc. for Computing Mach.*, vol. 2, pp. 28–29; September, 1959.

Early Chinese writings on the conception of binary numbers and octal diagrams are summarized. The basic element described is a trio of two-state symbols, having eight states in all. Its application to the representation of octal numbers in computers is suggested.

688
Central-European Computers, by N. M. Blachman (Office of Naval Res., U. S. Embassy, London); *Commun. Assoc. for Computing Mach.*, vol. 2, pp. 14–18; September, 1959.

Computer developments in East Germany, Czechoslovakia, Austria, and Yugoslavia are reviewed. The machines described are medium scale and slow speed, and tend to be technically unsophisticated. Operation times are generally measured in milliseconds and relays are copiously employed. Machines described in detail are the Zeiss-built ZRA 1, the Czech SAPO and the Austrian Mailüfterl ("gentle May breeze" in contrast to Whirlwind).

689
Specialist Discussion Meetings on New Digital-Computer Techniques 16th–17th February, 1959; *Proc. IEE (London)*, vol. 106, pt. B, pp. 444–469; September, 1959.

Summaries of some thirty papers presented at the Specialist Discussion Meetings on New Digital-Computer Techniques, February 16–17, 1959 are given. The papers deal with character recognition, peripheral equipment, low-temperature storage and switching devices, and special aspects of logical design.

690
The British Computer Society Conference, Cambridge, England, June 22–25, 1959 (Based on a report by the Society); *Computers and Automation*, vol. 8, pp. 12–15; September, 1959.

The proceedings of the British Computer Society Conference are summarized. Among the subjects discussed are British computers, training of programmers, accounting by computers, logical design, automatic programming, numerical analysis, and a variety of commercial and economic applications.

691
New Horizons in Computing; *Wireless World*, vol. 65, pp. 311–314; July–August, 1959.

The papers presented at the International Conference on Information Processing held recently at Paris are reviewed and the exhibits at the "Automath" Exhibition are described. The conference papers dealt with such subjects as engineering design of computers, mathematical methods, linear programming, and machine translation of languages. Papers dealing with microcircuitry and the parametron are discussed at length.

692
Survey of Progress and Trend of Development and Use of Automatic Data-Processing in Business and Management Control Systems of the Federal Government, as of December 1957—Part III; *Commun. Assoc. for Computing Mach.*, vol. 2, pp. 34–43; September, 1959.

The present scope and rate of expansion of the use of computers in the Federal Government are described. The biggest users are the armed forces where the most time-consuming applications are in logistics and supply. The computer issue of treasury checks and preparations for the 1960 Decennial Census are discussed. The cost and savings involved are generally reckoned in terms of increased availability of information rather than a significant reduction in personnel. The lack of a direct means of sensing of printed matter for computer input is a severe limitation on the expansion of computer applications in this field.

693
J.E.I.D.A. and its Computer Center; *Commun. Assoc. for Computing Mach.*, vol. 2, pp. 10–16; October, 1959.

The organization, purposes, and establishment of the Japanese Electronic Industry Development Association are outlined. Tabulated details of the four main commercially-produced Japanese computers are provided. These are the NEAC-2203, the HITAC-301 (both medium capacity all-transistorized drum-memory computers), the FACOM-212, and the TOSBAC-111, the latter two being compatible with punched card input.

SUBJECT INDEX

AUTHOR INDEX

PGEC News and Notices

EDITOR'S NOTE

This *News and Notice's* Section is open to all who have an announcement of a conference, symposium, session, publication, or other artifact of interest to the PGEC membership. Please send announcements to the *Editor*, who will put them in the first available issue. The right is reserved to edit the announcements, and to decide whether they indeed are aimed at our audience.

COMING MEETINGS

1960 WJCC

The date for the 1960 WJCC (Western Joint Computer Conference) is May 3–5. The place is San Francisco.

The theme of the Conference is "Computers—Challenge of the Next Decade," and special emphasis will be placed on areas in which substantial growth and development are anticipated during the 1960's, such as language translation, data retrieval, and self-teaching systems.

Proceedings will be distributed at the Conference.

1960 ELECTRONIC COMPONENTS CONFERENCE (EIA, AIEE, IRE, WCEMA)

Willard Hotel, Washington, D. C., May 10–12, 1960, are the space-time coordinates. For further information, write to Herbert H. Rosen, Publicity Chairman, National Aeronautics and Space Administration, 1520 H Street, N.W., Washington 25, D. C.

ONR SYMPOSIUM ON SUPERCONDUCTIVE TECHNIQUES FOR COMPUTING SYSTEMS

On May 17-19, 1960, the Information Systems Branch, Office of Naval Research, will sponsor a Symposium on Superconductive Techniques for Computing Systems. It will be held in the Department of the Interior Auditorium on C Street between 18th and 19th Streets, N.W., Washington, D. C. The program includes 29 papers covering diverse aspects of the cryogenics field, from the physics to the circuits. Programs and registration information may be obtained from:

Miss Josephine Leno
Code 430A
Office of Naval Research
Washington 25, D. C.
(Phone: OXford 6-6213)

CONFERENCE ON PARALLEL PROGRAMMING

The Cleveland-Akron Chapter of the ACM is sponsoring a Conference on Parallel Programming at the NASA Lewis Research Center Auditorium in Cleveland, Ohio, on Thursday, May 19, 1960. Attendance is by preregistration only. For registration details, call or write to L. R. Turner, Lewis Research Center, 21000 Brookpark Road, Cleveland 35, Ohio.

D.R.I. SEVENTH ANNUAL SYMPOSIUM ON COMPUTERS AND DATA PROCESSING

Denver Research Institute of the University of Denver is sponsoring its Seventh Annual Symposium on Computers and Data Processing on July 28–29, 1960. Three sessions are planned on components, logic design, and the philosophy of computer design. Write to W. H. Eichelberger, Arrangements Chairman, Denver Research Institute, Denver 10, Colo., for all details. (Colorado is very pleasant in July—*Editor's comment.*)

ANNUAL ACM MEETING

The fifteenth Annual Meeting of the Association for Computing Machinery will be held at Marquette University, Milwaukee, Wis., on August 23–25, 1960. Local arrangements will be under the direction of Prof. Arthur Moeller of Marquette. Contributed and invited papers on all phases of analog and digital computation, business applications, and data processing will be presented. Round-table discussions and a "Hall of Discussions" are planned.

WESCON

August 23–26, in Los Angeles.

INTERNATIONAL SYMPOSIUM ON DATA TRANSMISSION

The Benelux Section of IRE is sponsoring an International Symposium on Data Transmission in Delft, The Netherlands, on September 19–20, 1960. The symposium will be concerned with the problems of transmitting and receiving information in digital form. Particular emphasis will be placed on the behavior of practical communication networks, including existing telephone systems, existing and planned military systems, and schemes of the future, such as those that use satellites. The aim of the symposium will be to reduce the gap now existing between theory and practice. The symposium will be conducted in English. The papers scheduled give a good representation of work being carried on the U.S. as well as in Europe. For further information, contact B. B. Barrow, Secretary, IRE Benelux Section, Postbus 14, Den Haag, The Netherlands.

AIEE SYMPOSIUM ON SWITCHING CIRCUIT THEORY AND LOGICAL DESIGN

The symposium will consist of sessions held during the AIEE Fall General Meeting in Chicago, October 9–14, 1960. For further information, write to Thomas H. Mott, Jr., RCA Laboratories, Princeton, N. J.

POWER INDUSTRY COMPUTER APPLICATIONS CONFERENCE

The Second Power Industry Computer Applications Conference sponsored by AIEE will be held in St. Louis, November 9–11, 1960. Complete details are available from E. L. Harder, Analytical Department 4113, Westinghouse Electric Corp., East Pittsburgh, Pa.

EJCC

New York, N. Y., December, 1960.

UNIVERSITY SUMMER PROGRAMS

Three short summer courses of interest to computer people have come to our attention. We are sure that this list is not exhaustive, but we suspect it is representative:

1) University of Michigan, June 13–24. Five courses in computer science and engineering (plus many others): introduction to digital computer engineering; theory of computing machine design; introduction to standard methods of numerical analysis; advanced numerical analysis; and programming concepts, automata, and adaptive systems. Write to Engineering Summer Conferences Office, 126 West Engineering Building, University of Michigan, Ann Arbor, Mich.

2) Massachusetts Institute of Technology, June 14–24. One course, switching circuits, supervised by Prof. Samuel H. Caldwell. Write to Office of the Summer Session, Room 7-103, M.I.T., Cambridge 39, Mass.

3) The Moore School of Electrical Engineering, University of Pennsylvania, June 20–July 16. Two courses in the computer field, one in numerical analysis supervised by Prof. Saul Gorn, the other on new devices in amplifying and switching, supervised by Prof. Noah Prywes. Courses are six hours per day, five days per week in air-conditioned rooms. Visiting lecturers as well

University faculty will participate. Write ecial Summer Session Office, The Moore hool of Electrical Engineering, 200 South d Street, Philadelphia 4, Pa.

BLICATIONS AVAILABLE

MPOSIUM ON THE MECHANIZA-ON OF THOUGHT PROCESSES

British Information Services reports that proceedings of the Symposium on the echanization of Thought Processes, held at National Physical Laboratory, England, November 24–27, 1958, is now available- $9.29 postpaid. The symposium included papers covering a wide range of topics in areas of artificial intelligence, automatic ogramming, mechanical language translan, speech recognition, learning in maines, neural nets and their implications biology, and the implication of all this industry. Authors are from Great itain, U.S., France, U.S.S.R., Israel, and ngary. Write to British Information rvices, 45 Rockefeller Plaza, New York, Y.; in Great Britain, write to Her ajesty's Stationery Office.

ROCEEDINGS OF THE 1959 UNESCO NTERNATIONAL CONFERENCE ON NFORMATION PROCESSING

The papers presented at the Paris Conence held June 15–20, 1959, are now in int as the *Proceedings of the International nference on Information Processing*. The ice is $25.00 per copy. Write to Columbia niversity Press, New York 27, N. Y., or NESCO Publications Center, 801 Third venue, New York 22, N. Y.

OMPUTER ABSTRACTS JOURNAL ND COMPUTING REVIEWS

Computer Abstracts is the new title of e bibliographic journal published by Techcal Information Company, Chancery ouse, Chancery Lane, London WC2, Engnd. The new letterpress journal replaces e duplicated *Computer Bibliography* forerly purveyed by the Company.

ACM has begun a new journal *Computg Reviews* under the editorship of Dr. hn W. Carr III, It will appear initially as section of *Communications of the ACM*, nd will feature critical reviews of a wide nge of computer books and papers.

CALL FOR PAPERS

COMPUTER ISSUE OF PROCEEDINGS OF THE IRE

The Institute of Radio Engineers will publish a special Computer Issue of PROCEEDINGS in January, 1961.

You are invited to submit a paper for publication in this issue. Papers on *new developments* in digital and analog computers are desired, especially in the following areas:

- Components
- Storage devices and systems
- Arithmetic, logic, and control elements, including self-organizing machines
- Input and output elements, including voice and pattern recognition, and displays
- Logical design, including use of computers in logical design
- Circuit design, including use of computers in circuit design
- General-purpose computers and data processors
- Computers optimized for special roles
- Large systems in which computers play a role
- Digital communication
- Microminiaturization.

The deadline for papers is July 29, 1960. Papers must include a 100-word abstract. Three copies of the paper and illustrations are required. Also include one set of illustrations that are reproducible, and photographs and biographies of the authors. They should be sent to E. K. Gannett, Managing Editor, 1 East 79th Street, New York 21, N. Y. Clearly indicate that the paper is intended for the Computer Issue.

Computer Issue Editorial Board: H. T. Larson, L. C. Hobbs, K. W. Uncapher.

PGEC CHAPTER ACTIVITIES

PGEC CHAPTER BIBLIOGRAPHY PROJECT

The PGEC announces a Chapter Bibliography Project. Chapters are invited to undertake the preparation of special-purpose bibliographies on advanced topics in the computer field, for publication in these TRANSACTIONS. For further information, contact Dr. L. F. Jones, Westinghouse Electric Corp., Air Arm 454, Box 746, Baltimore 3, Md.

BOSTON CHAPTER ORGANIZES DISCUSSION GROUPS

Informal discussion groups have been organized on a trial basis by the Boston Chapter of the PGEC. Four groups were started, each covering a specific area in the computer field. For example, one group centers on the design considerations of automatic programming systems.

The support is enthusiastic, and two of the groups meet regularly. The size of the group and the nature of the discussion appear to depend primarily on the discussion leader and secondarily on the topic. Groups have ranged in size from six to over twenty; the smaller groups permit more participation.

These groups fill a definite need that is not satisfied by the usual technical papers sponsored by the Chapter. It is planned to continue and extend this activity in the Fall.

PHILADELPHIA CHAPTER PLANS MEETING IN MAY

The Philadelphia Chapter will hold its its final meeting of 1959–1960 on May 11 at the Cherry Hill RCA plant. The program will consist of a panel discussion on "Operating Experience with Solid-State Computers," and will include panel members from RCA, Remington Rand Univac, and Philco. In addition, election of officers for the coming year will be conducted. Nominees are: William E. Bradley (Philco) for Chairman; Robert A. C. Lane (RCA) for Vice Chairman; George Lund (Burroughs) for Secretary.

Peter E. Raffa (Technitrol), Irv Glassman (RCA), Lester Spandorfer (Remington Rand Univac), Robert Tillman (Burroughs), and Jerry Conklin (GE) are nominated for Administrative Committee posts.

PHILADELPHIA SYMPOSIUM

IRE, AIEE AND SIAM (Society for Industrial and Applied Mathematics) have cooperated to give a seven-lecture Symposium on Computer Applications for Engineers, on Monday evenings from February 29 through April 18 in Philadelphia. Attendance has averaged over 80 for the lectures to date, and the papers have been well received.

INFORMATION FOR AUTHORS

IRE TRANSACTIONS ON ELECTRONIC COMPUTERS is published quarterly, in March, June, September, and December, with a distribution of over 9000 copies, largely to engineers, logicians, and supervisors in the computer field. Its scope includes the design, theory, and practice of electronic computers and data-processing machines, digital and analog, and parts of certain related disciplines such as switching theory and pulse circuits.

If a paper of widespread interest beyond the computer field is submitted, it will be recommended to the Editor of PROCEEDINGS OF THE IRE for publication. If our reviewers feel that a paper should be submitted to a different IRE TRANSACTIONS, we will so recommend to the author.

Publication time in IRE TRANSACTIONS ON ELECTRONIC COMPUTERS, from receipt of the original manuscript to mailing of the issue, is normally in excess of 5 months, but can be made as little as $3\frac{1}{2}$ months if the occasion demands and the manuscript is carefully prepared.

To avoid delay, please be guided by the following suggestions:

A. Process for Submission of a Technical Paper

1) Send to the Editor three copies of your manuscript, each copy complete with illustrations. (For Letters to the Editor, two copies will do.)

2) Enclose originals for the illustrations, in the style described below. Alternatively, be ready to send the originals immediately upon acceptance of the paper.

3) Enclose a separate sheet giving your preferred address for correspondence and return of proofs.

4) Enclose a technical biography and photograph of each author, or be ready to supply these upon acceptance of the paper. For biography style, see any IRE journal.

5) If the manuscript has been presented, published, or submitted for publication elsewhere, please so inform the Editor. Our primary objective is to publish technical material not available elsewhere, but on occasion we publish papers of unusual merit that have appeared or will appear before other audiences.

B. Style for Manuscript

1) Typewrite, double or $1\frac{1}{2}$ space; use one side of sheet only. (Good office-duplicated copies are acceptable.)

2) Provide an informative 100- to 250-word summary (abstract) at the head of the manuscript. It will appear with the paper and also separately in PROCEEDINGS OF THE IRE.

3) Provide a separate double-spaced sheet listing all footnotes, beginning with "*Manuscript received by the PGEC _____," and "†(Affiliation of author)," and continuing with numbered references. Acknowledgment of financial support is often placed at the end of the asterisk footnote.

4) Give complete references, insofar as possible. See footnotes in this or previous issues for examples of IRE style. References will be printed as footnotes in the column where first mentioned.

5) You may choose to provide a "Bibliography" at the end of the paper, with items referred to by a numeral in square brackets, *e.g.*, [12], to supplement or supplant footnote references.

6) Provide a separate sheet listing all figure captions, in proper style for the typesetter, *e.g.*: "Fig. 1—Example of a disjoint and distraught manifold."

C. Style for Illustrations

1) Originals for illustrations should be sharp, noise-free, and of good contrast. We regret that we cannot provide drafting or art service.

2) Line drawings should be in India ink on drafting cloth, paper, or board. Use $8\frac{1}{2} \times 11$ inch size sheets if possible, to simplify handling of the manuscript.

3) On graphs, show only the coordinate axes, or at most the major grid lines, to avoid a dense, hard-to-read result.

4) All lettering should be large enough to permit legible reduction of the figure to column width, perhaps as much as 4:1.

5) Photographs should be glossy prints, of good contrast and gradation, and any reasonable size.

6) Number each original on the back, or at the bottom of the front.

7) Note item B-6 above. Captions lettered on figures will be blocked out in reproduction, in favor of typeset captions.

Dr. Howard E. Tompkins, *Editor*
IRE TRANSACTIONS ON ELECTRONIC COMPUTERS

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